

System Block Diagram

SYNC_MASTER=DEREK

SYNC_DATE=1/19/2007

NOTICE OF PROPRIETARY PROPERTY

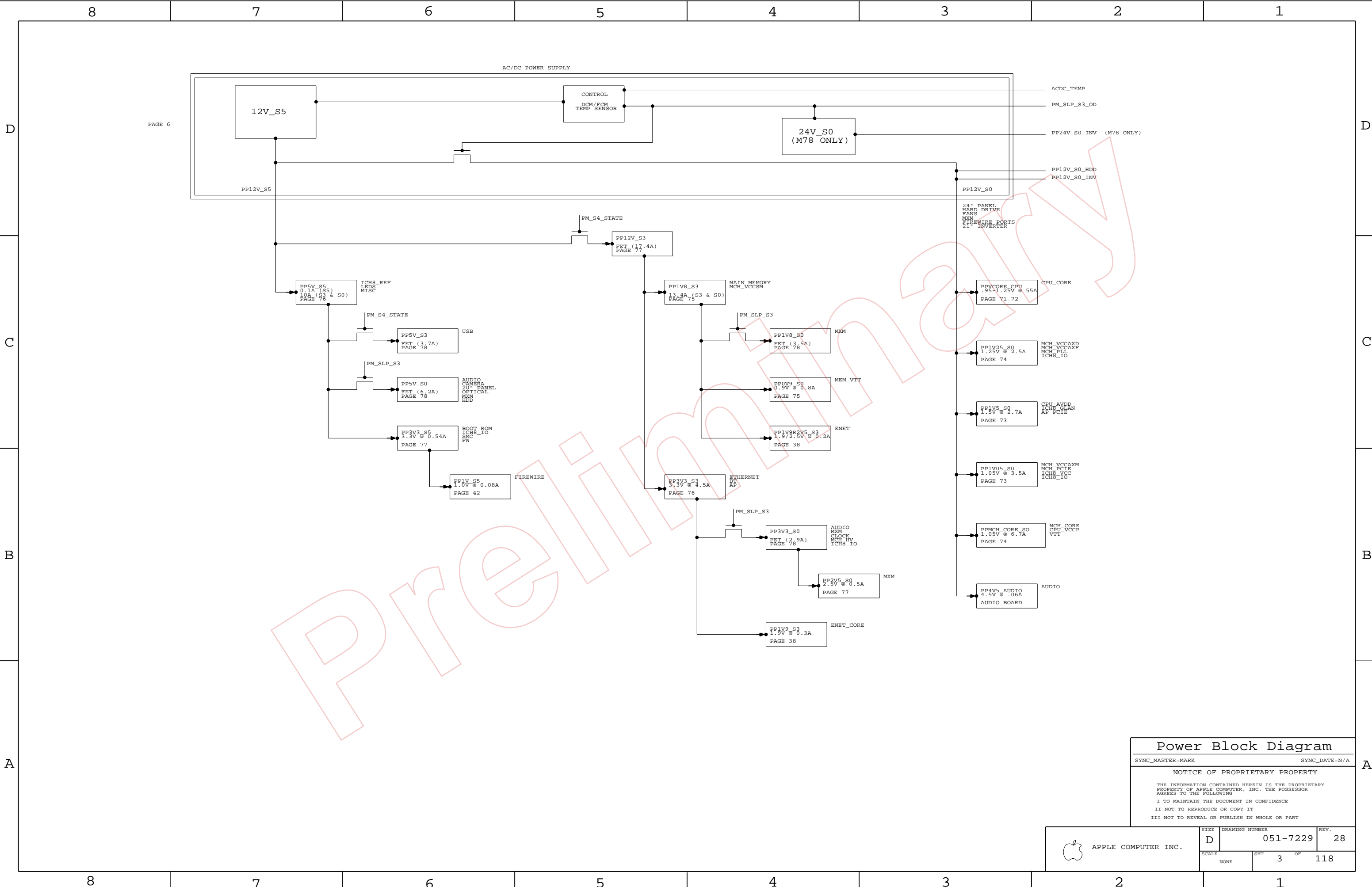
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7229	28
SCALE		SHT	OF
NONE		2	118



Power Block Diagram

SYNC_MASTER=MARK

SYNC_DATE=N/A

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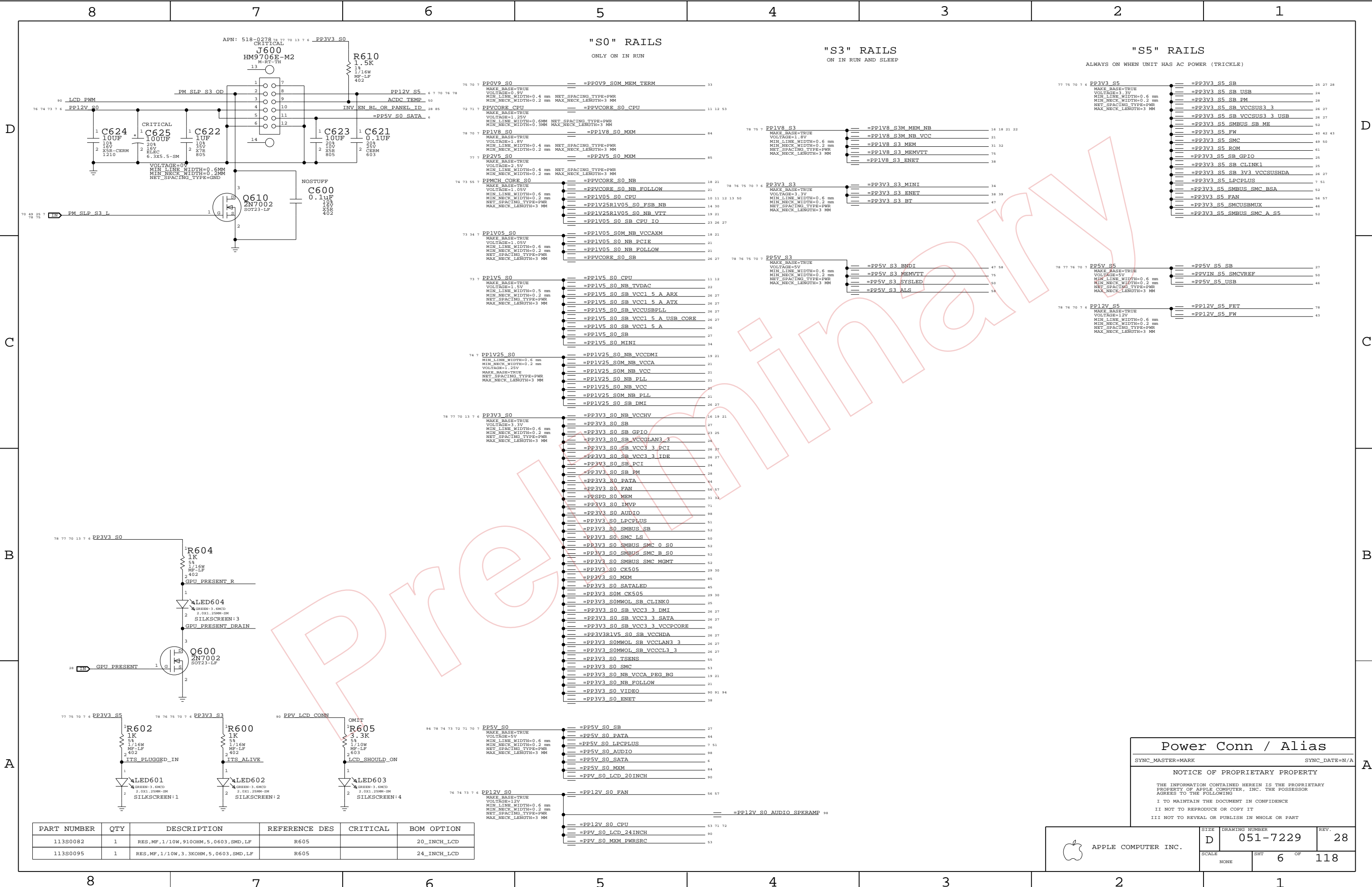
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	D	051-7229	28
SCALE		SHT	OF
NONE		3	118

8		7		6		5		4		3		2		1		
BOM Variants																
BOM NUMBER		BOM NAME				BOM OPTIONS										
630-7977		PCBA,MLB,M78,CTO,2.8G				24_INCH_LCD,2P8GHZ_CPU,BASIC,CR_E,V8										
630-7976		PCBA,MLB,M78,BTR,2.4G				24_INCH_LCD,2P4GHZ_CPU,BASIC,CR_STD,V6										
630-7875		PCBA,MLB,M78,CTO,2.2G				24_INCH_LCD,2P2GHZ_CPU,BASIC,CR_STD,V6										
607-0429		M78 DEVELOPMENT				CPU_TDIODE,DEVELOPMENT,XDP_CONN,LIT_IO,LPCPLUS,MXM_PWR_SENSE										
630-7979		PCBA,MLB,M72,CTO,2.4G				20_INCH_LCD,2P4GHZ_CPU,BASIC,CR_STD,V6										
630-7978		PCBA,MLB,M72,BTR,2.2G				20_INCH_LCD,2P2GHZ_CPU,BASIC,CR_STD,V6										
630-7874		PCBA,MLB,M72,GD,2.0G				20_INCH_LCD,2P0GHZ_CPU,BASIC,CR_STD,V6										
607-0462		M72 DEVELOPMENT				CPU_TDIODE,DEVELOPMENT,ITP_CONN,LIT_IO,LPCPLUS,MXM_PWR_SENSE										
BOM GROUPS																
BOM GROUP		BOM OPTIONS														
BASIC		5V1V8REG_SKIP,ALTERNATE,COMMON,ITP/XDP,MXM_ROM,NBCFG_PEG_REVERSE,YUKON_ULTRA														
V6		LOW_TDP														
V8		HIGH_TDP														
Bar Code Labels / EEE #'s																
PART NUMBER		QTY	DESCRIPTION				REFERENCE DES		CRITICAL		BOM OPTION					
Module Parts																
PART NUMBER		QTY	DESCRIPTION				REFERENCE DES		CRITICAL		BOM OPTION					
COMMON																
PART#		QTY	DESCRIPTION				REFERENCE DESIGNATOR(S)		CRITICAL		BOM OPTION					
338S0430		1	IC,NB,CRESTLINE,PM,C0,QS				U1400		CRITICAL							
338S0427		1	IC,SB,ICH8M,B1,QS				U2300		CRITICAL							
359S0130		1	CK505 - SILEGO SLG2AP101				U2900		CRITICAL							
820-2149		1	PCB,FAB,IO ALIGNMENT,M72				IO1		CRITICAL							
069-2046		1	M72/M78 22UF CAP INTERCHANGEABILITY				DOC1									
825-6447		1	MLB LABEL,48.0X4.8				X14		CRITICAL							
341S1892		1	IC,2K I2C EEPROM,MXM				U8570		CRITICAL		MXM_ROM					
337S3438																
337S3438		1	IC,MDC,SR,E1,QS,2.8G,55W,800FSB,4M,PDA				CPU		CRITICAL		2P8GHZ_CPU					
337S3436		1	IC,MDC,SR,E1,QS,2.6G,45W,800FSB,4M,PDA				CPU		CRITICAL		2P6GHZ_CPU					
337S3435		1	IC,MDC,SR,E1,QS,2.4G,35W,800FSB,4M,PDA				CPU		CRITICAL		2P4GHZ_CPU					
337S3461		1	IC,MDC,SR,E1,QS,2.2G,35W,800FSB,4M,PDA				CPU		CRITICAL		2P2GHZ_CPU					
337S3460		1	IC,MDC,SR,E1,QS,2.0G,35W,800FSB,4M,PDA				CPU		CRITICAL		2P0GHZ_CPU					
337S3437																
337S3437			337S3436				CPU		CPU,2.6G,55W							
124-0361			124-0339				C7490,C7491		CAP							
371S0464			371S0154				D7624,D7664		DIODES							
MXM_PWR_SENSE BOMOPTION CHANGE FOR PRODUCTION																
PART#		QTY	DESCRIPTION				REFERENCE DESIGNATOR(S)		CRITICAL		BOM OPTION					
107S0070		1	RES,0-OHM,2512				R5350				PRODUCTION					
116S0090		2	RES,10K-OHM,5%,0402				C5358,C5359				PRODUCTION					
BOM Configuration																
SYNC_MASTER=JAMES SYNC_DATE=10/16/06																
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												SCALE NONE		SHT 4	OF 118	
8		7		6		5		4		3		2		1		



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
113S0082	1	RES, MF, 1/10W, 9100HM, 5, 0603, SMD, LF	R605		20_INCH_LCD
113S0095	1	RES, MF, 1/10W, 3, 3KOHM, 5, 0603, SMD, LF	R605		24_INCH_LCD

Power Conn / Alias

SYNC_MASTER=MARK

SYNC_DATE=N/A

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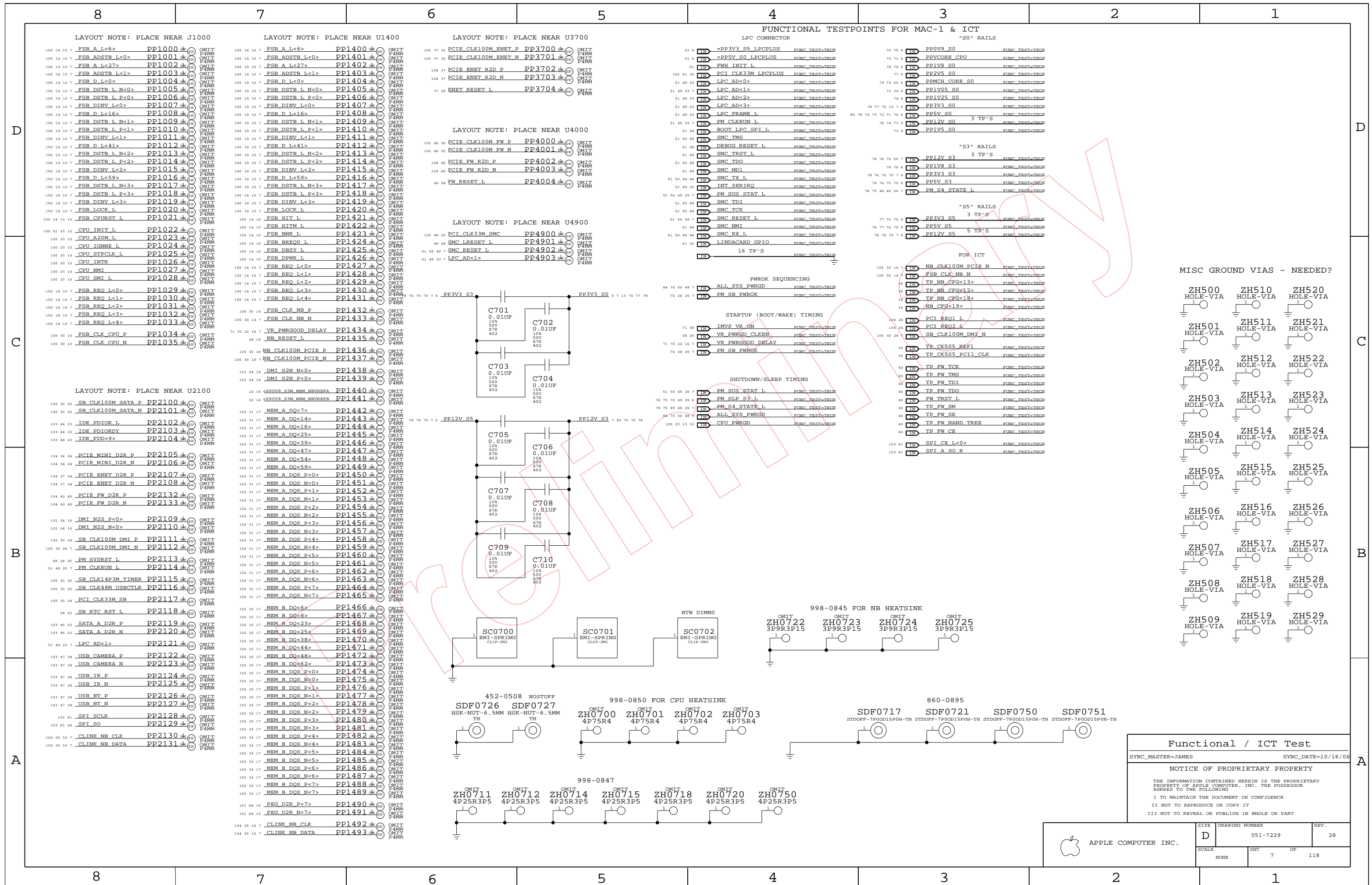
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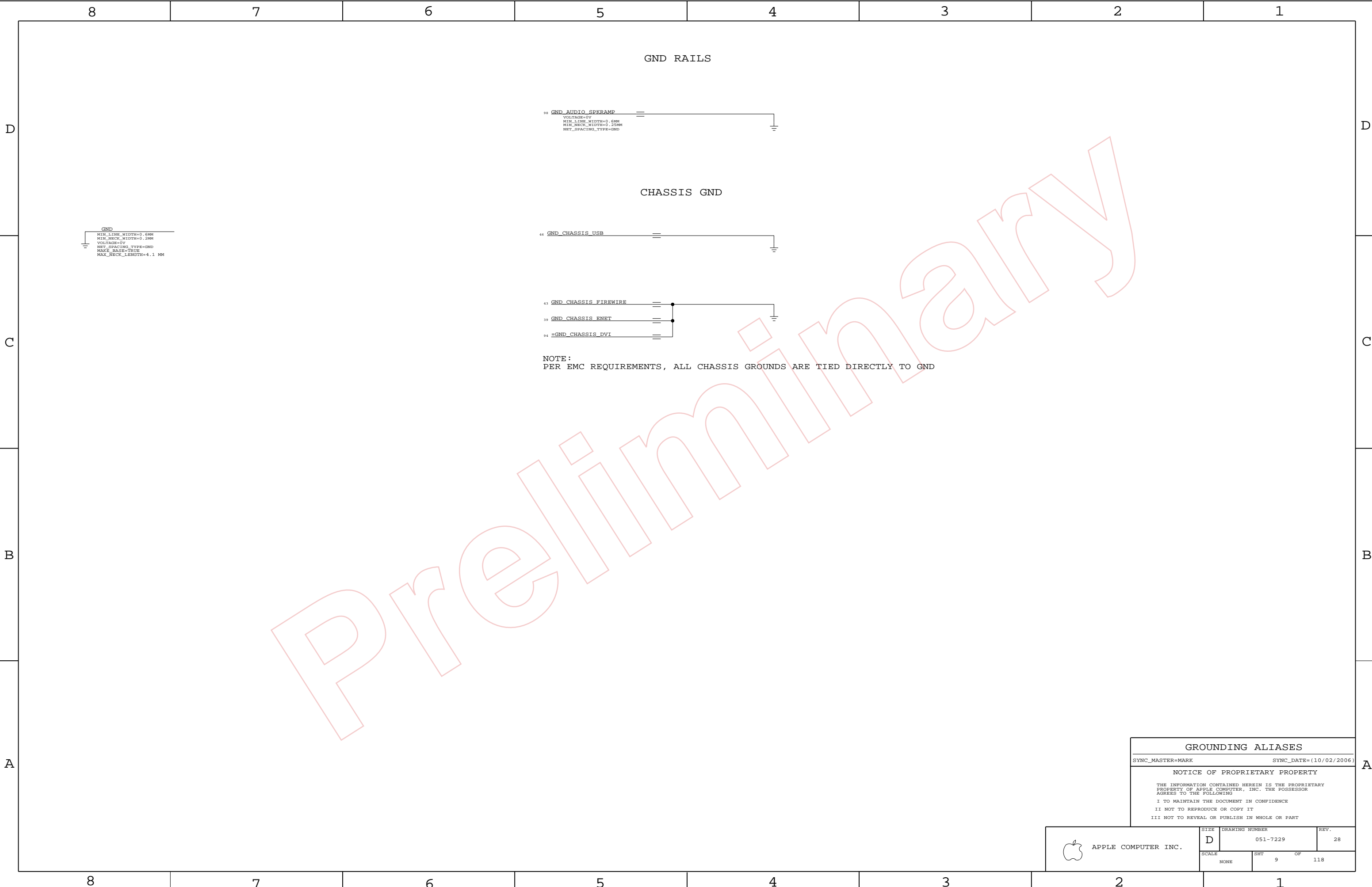
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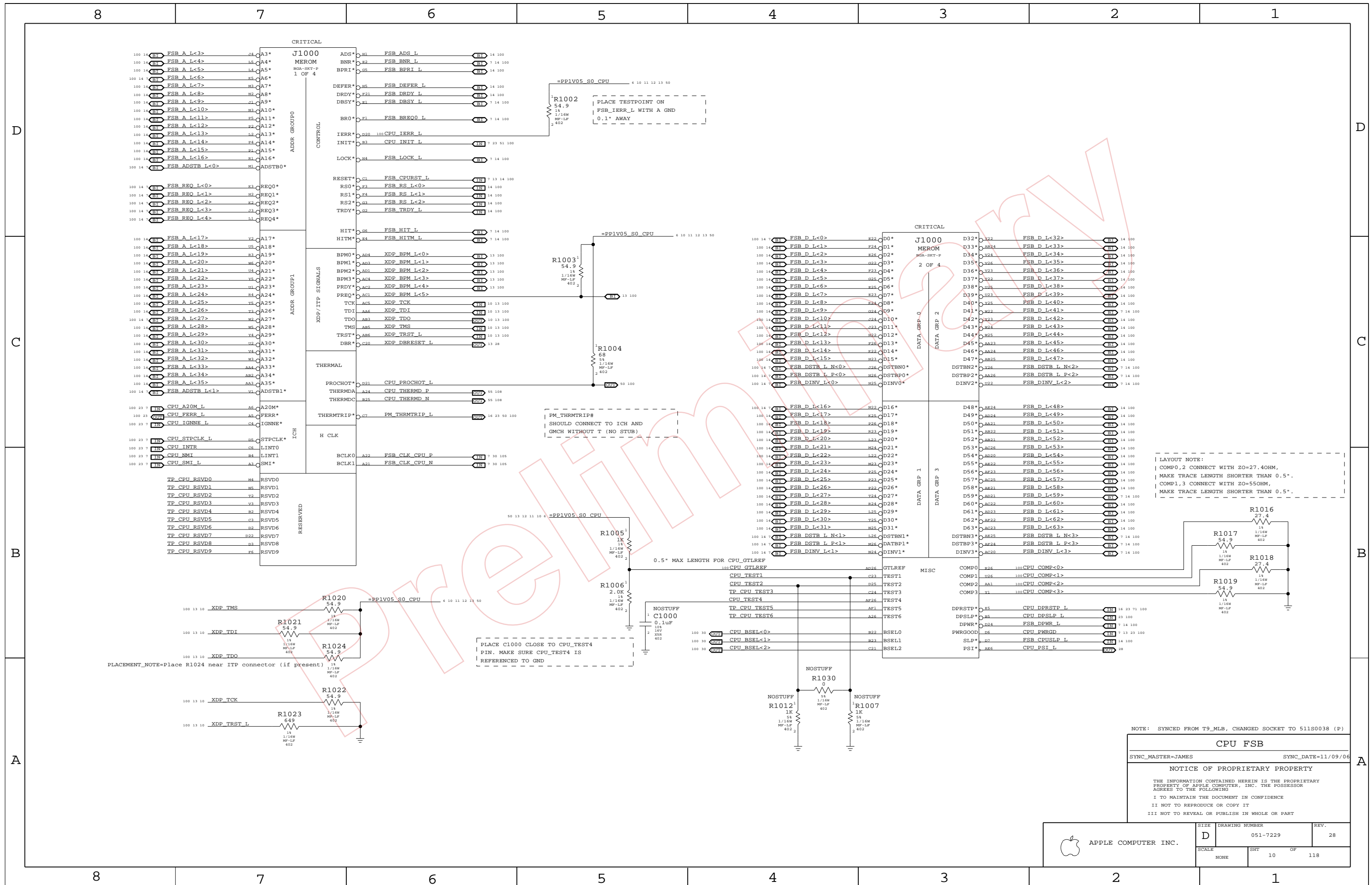
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SCALE		SHT	OF
NONE		6	118







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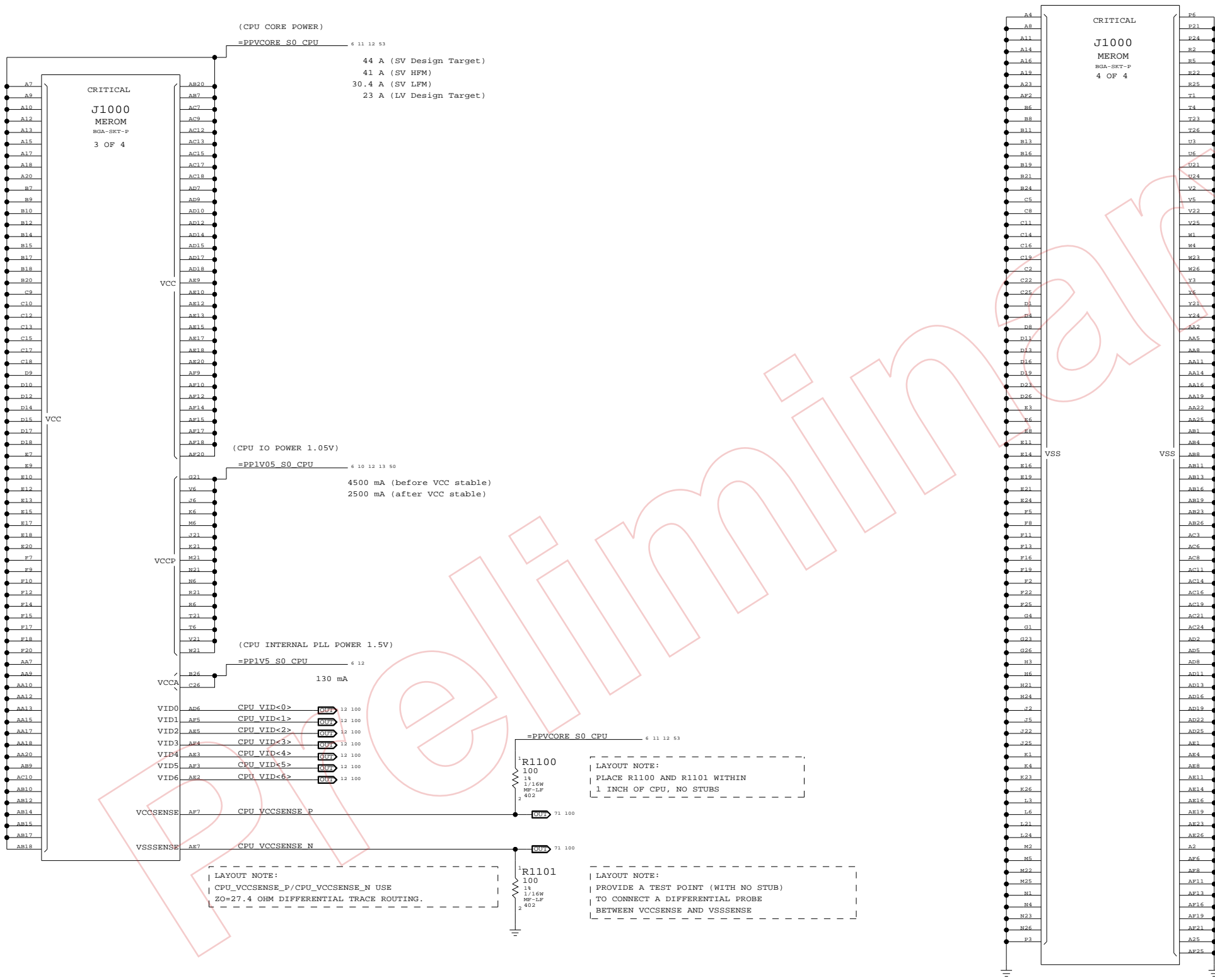
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LAYOUT NOTE:
PLACE R1100 AND R1101 WITHIN
1 INCH OF CPU, NO STUBS

LAYOUT NOTE:
CPU_VCCSENSE_P/CPU_VCCSENSE_N USE
Z0=27.4 OHM DIFFERENTIAL TRACE ROUTING.

LAYOUT NOTE:
PROVIDE A TEST POINT (WITH NO STUB)
TO CONNECT A DIFFERENTIAL PROBE
BETWEEN VCCSENSE AND VSSSENSE

NOTE: SYNCED FROM T9_MLB, CHANGED SOCKET TO 511S0038 (P)

CPU Power & Ground

SYNC_MASTER=JAMES SYNC_DATE=11/09/06

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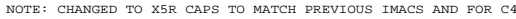
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SCALE		SHT	OF
NONE		11	118

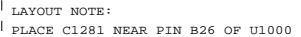
6X 220UF. 32X 22UF 0805



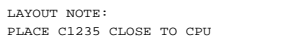
Resistors to allow for override of CPU VID
Will probably be removed before production




VCCA (CPU AVdd) DECOUPLING



VCCP (CPU I/O) DECOUPLING



 APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
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	SCALE	SHT	OF
	NONE	12	118

Mini-XDP Connector

NOTE: This is not the standard XDP pinout.
Use with 920-0451 adapter board to support CPU, NB & SB debugging.

Direction of XDP module
Please avoid any obstructions
on even-numbered side of J1300

eXtended Debug Port (XDP)			
SYNC_MASTER=T9_MLB_NAME		SYNC_DATE=11/06/2006	
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D	051-7229	28

APPLE COMPUTER INC.

SCALE	SHT	OF	118
NONE	13		

8 7 6 5 4 3 2 1

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8 7 6 5 4 3 2 1

Mini-XDP Connector

NOTE: This is not the standard XDP pinout.
Use with 920-0451 adapter board to support CPU, NB & SB debugging.

Direction of XDP module
Please avoid any obstructions
on even-numbered side of J1300

eXtended Debug Port (XDP)			
SYNC_MASTER=T9_MLB_NOME		SYNC_DATE=11/06/2006	
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SCALE NONE SHT 13 OF 118

8 7 6 5 4 3 2 1

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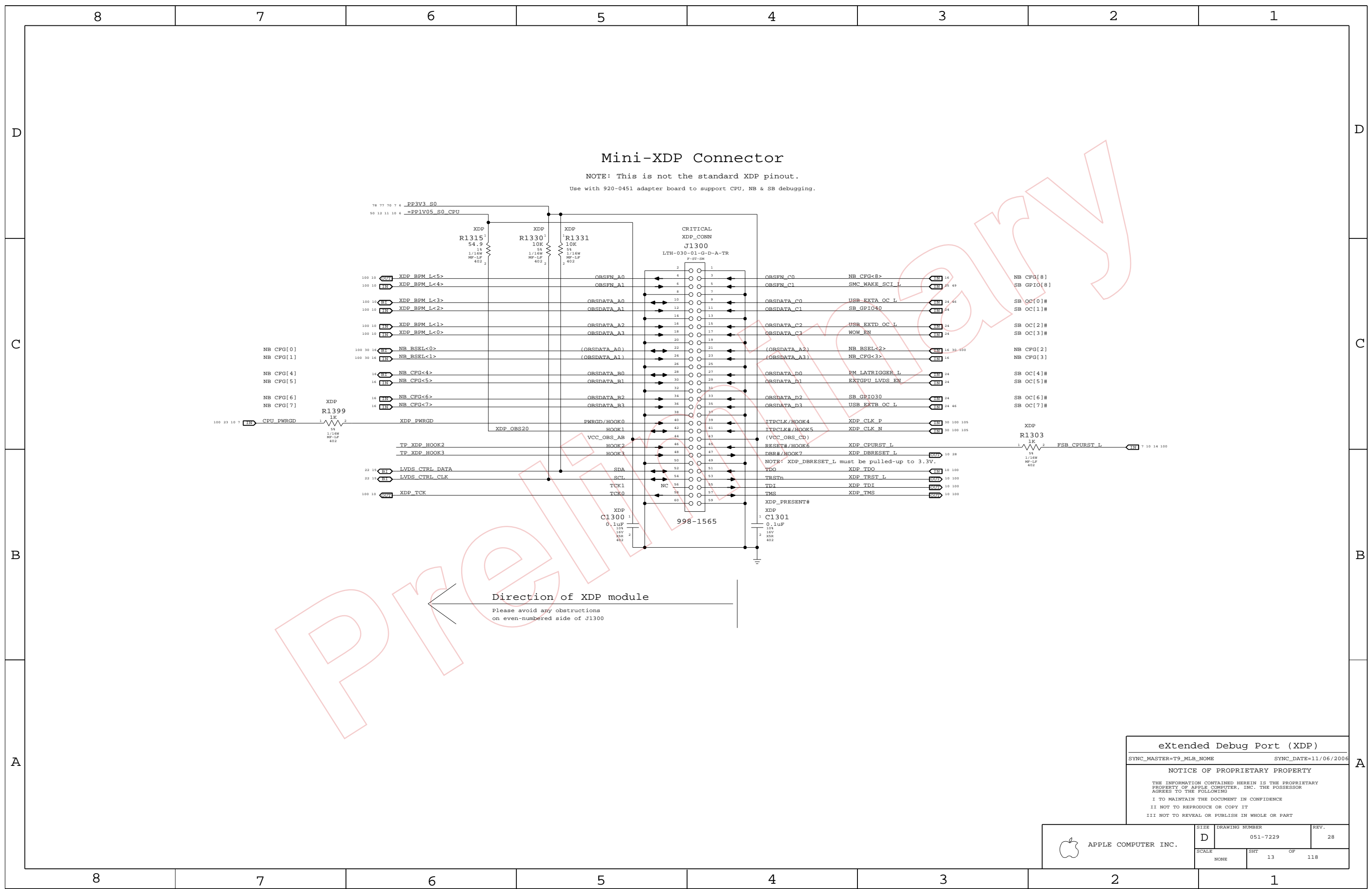
Direction of XDP module
Please avoid any obstructions
on even-numbered side of J1300

eXtended Debug Port (XDP)			
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SCALE NONE SHT 13 OF 118

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Mini-XDP Connector

NOTE: This is not the standard XDP pinout.
Use with 920-0451 adapter board to support CPU, NB & SB debugging.

The diagram illustrates the Mini-XDP Connector circuit. It features a central J1300 connector (LTH-030-01-G-D-A-TR) with 60 pins. Various components are connected to these pins, including resistors (R1315, R1330, R1331, R1399, R1303), capacitors (C1300, C1301), and logic components like the CPU PWRGD, NB CFG, and SB GPIO. The diagram also shows connections for XDP module signals such as XDP_BPM, XDP_OBS20, XDP_PWRGD, XDP_OBS20, XDP_CLK_P, XDP_CLK_N, XDP_CPURST_L, XDP_DBRESET_L, XDP_TDO, XDP_TRST_L, XDP_TDI, XDP_TMS, and XDP_PRESENT#. A large 'PRELIMINARY' watermark is overlaid on the diagram. A note at the bottom indicates the direction of the XDP module and advises avoiding obstructions on the even-numbered side of J1300.

Direction of XDP module
Please avoid any obstructions
on even-numbered side of J1300

eXtended Debug Port (XDP)			
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SCALE	SHT	OF	118
NONE	13	OF	118

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Mini-XDP Connector

NOTE: This is not the standard XDP pinout.
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The diagram illustrates the Mini-XDP Connector circuit. It features a central J1300 connector (LTH-030-01-G-D-A-TR) with 60 pins. Various components are connected to these pins, including resistors (R1315, R1330, R1331, R1399, R1303), capacitors (C1300, C1301), and logic components like the CPU PWRGD, NB CFG, and SB GPIO. The diagram also shows connections for XDP module signals such as XDP_BPM, XDP_OBS20, XDP_PWRGD, XDP_OBS20, XDP_CLK_P, XDP_CLK_N, XDP_CPURST_L, XDP_DBRESET_L, XDP_TDO, XDP_TRST_L, XDP_TDI, XDP_TMS, and XDP_PRESENT#. A large 'PRELIMINARY' watermark is overlaid on the diagram. A note at the bottom indicates the direction of the XDP module and advises avoiding obstructions on the even-numbered side of J1300.

Direction of XDP module
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on even-numbered side of J1300

eXtended Debug Port (XDP)			
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NONE	13	OF	118

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Mini-XDP Connector

NOTE: This is not the standard XDP pinout.
Use with 920-0451 adapter board to support CPU, NB & SB debugging.

Direction of XDP module
Please avoid any obstructions
on even-numbered side of J1300

eXtended Debug Port (XDP)

SYNC_MASTER=T9_MLB_NOME SYNC_DATE=11/06/2006

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SIZE D DRAWING NUMBER 051-7229 REV. 28

SCALE NONE SHT 13 OF 118

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Mini-XDP Connector

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Use with 920-0451 adapter board to support CPU, NB & SB debugging.

Direction of XDP module
Please avoid any obstructions
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eXtended Debug Port (XDP)			
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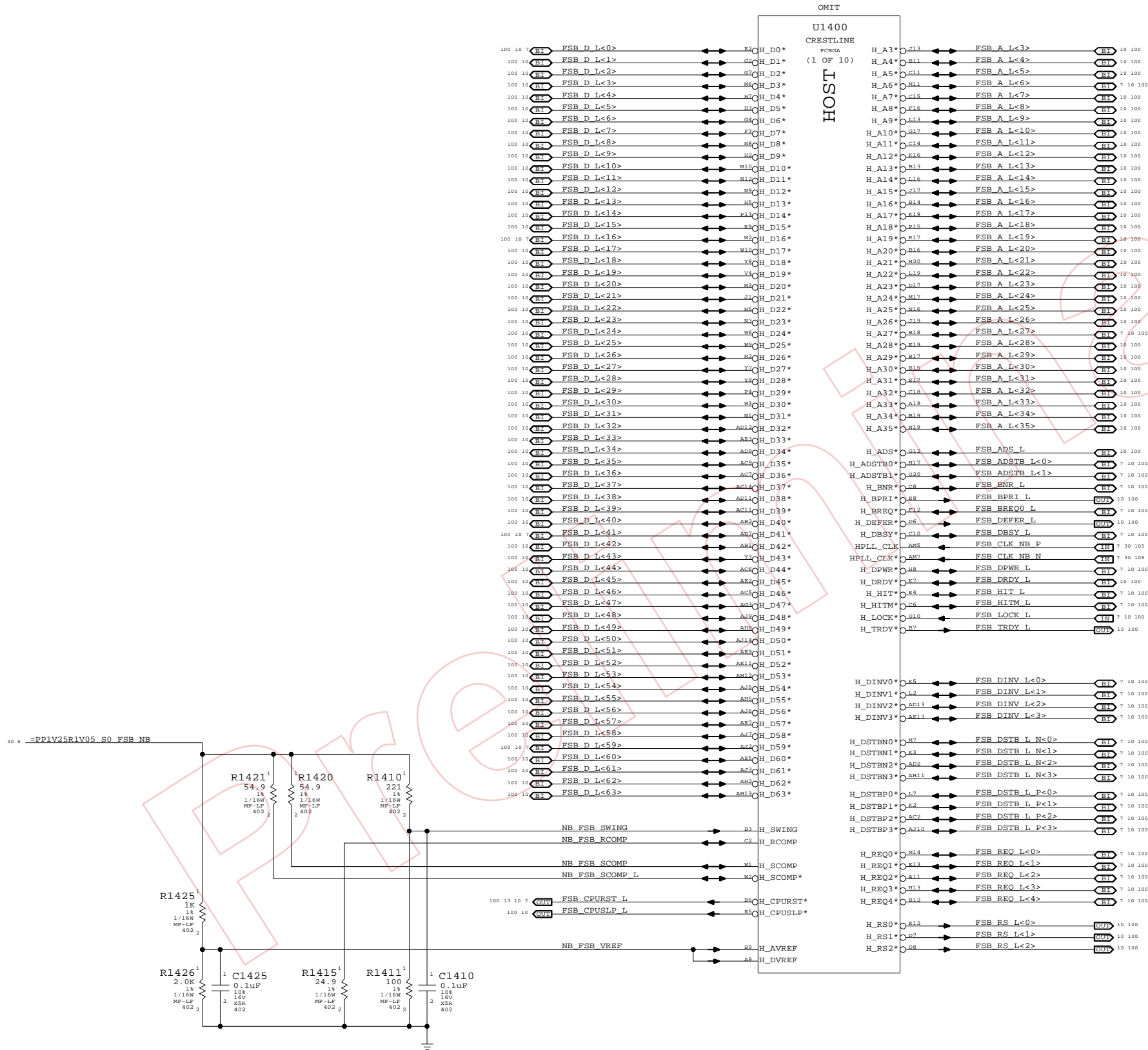
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NB CPU Interface

SYNC_MASTER=T9_MLB SYNC_DATE=10/30/2006

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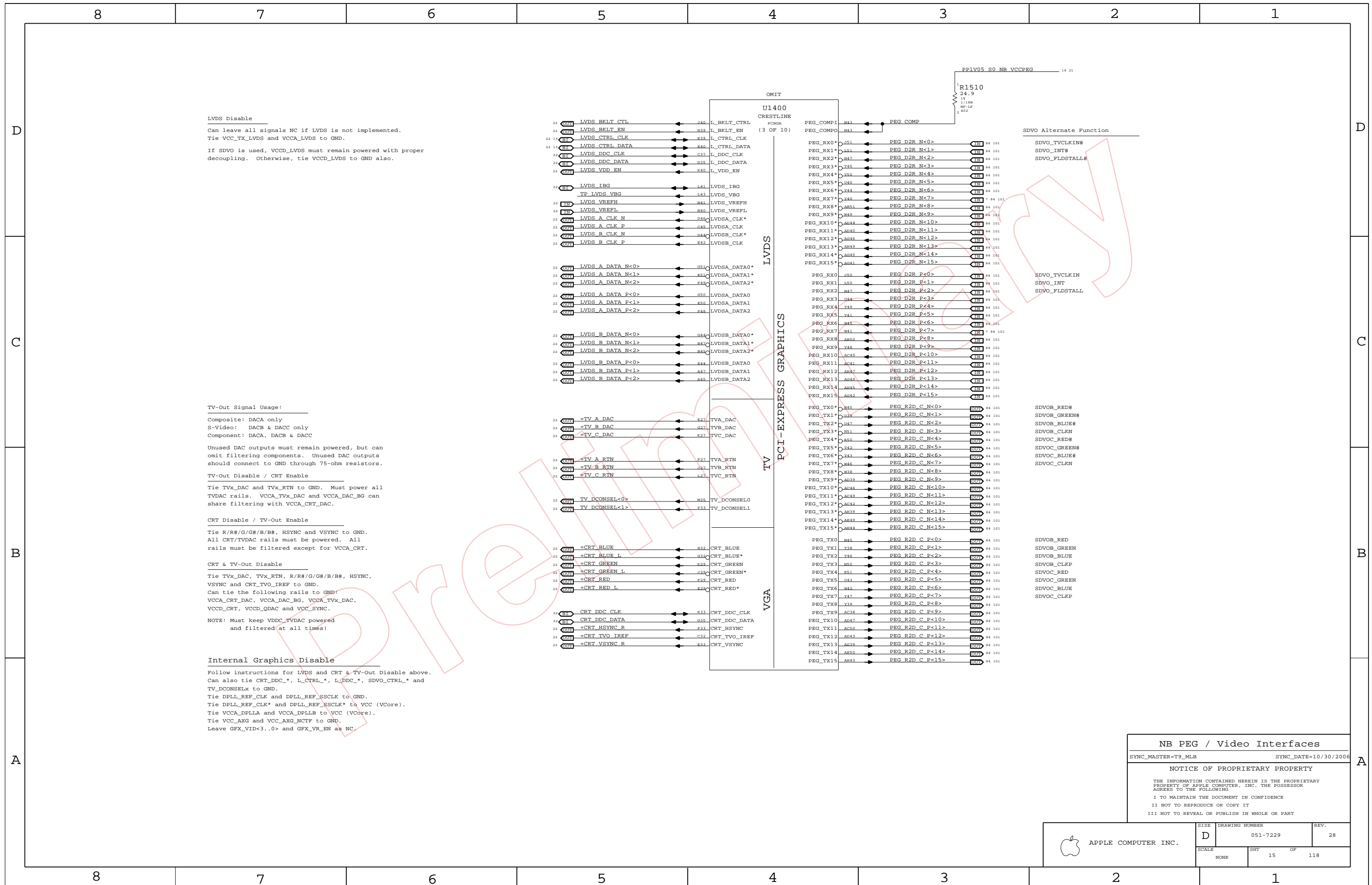
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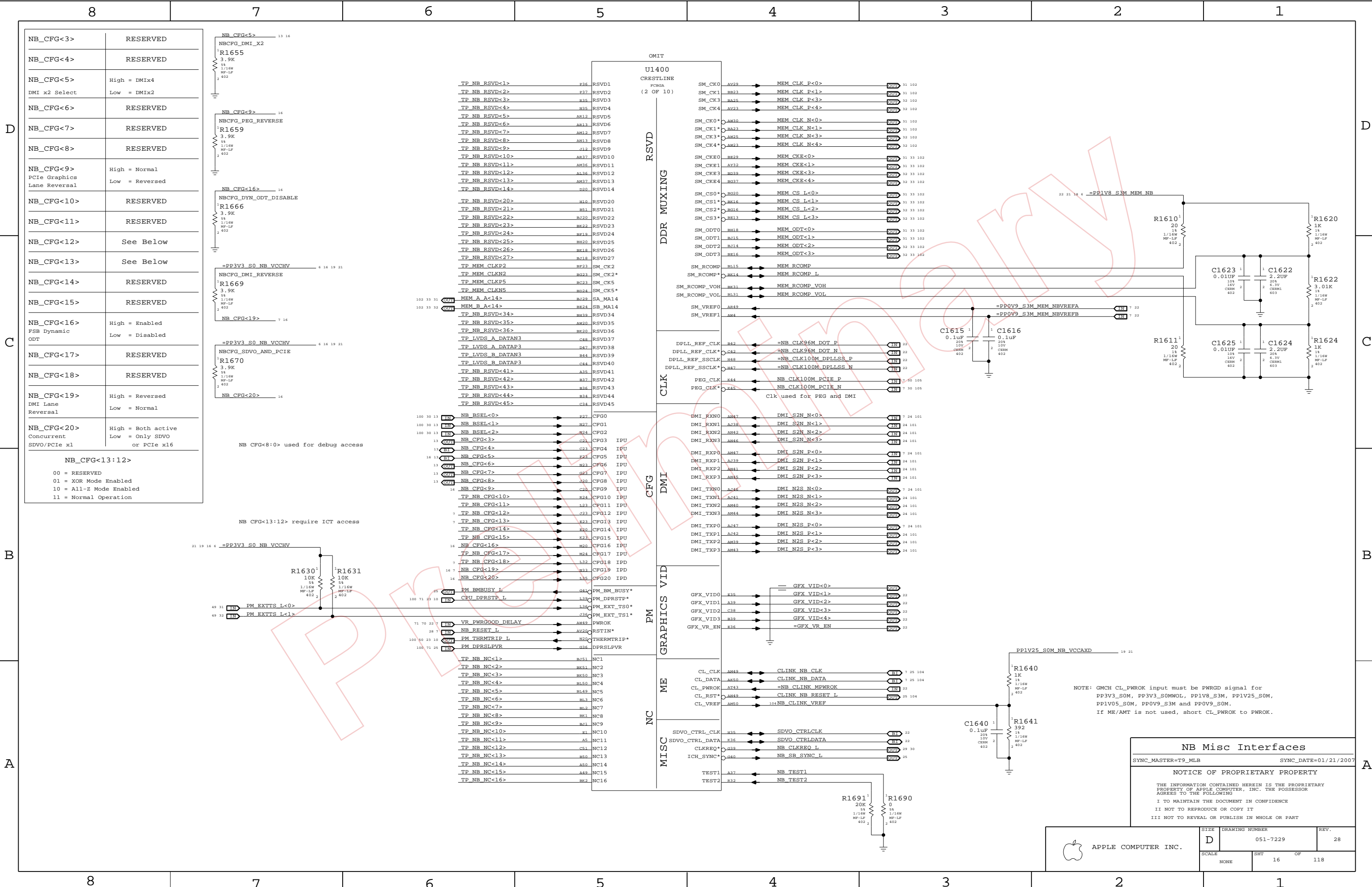
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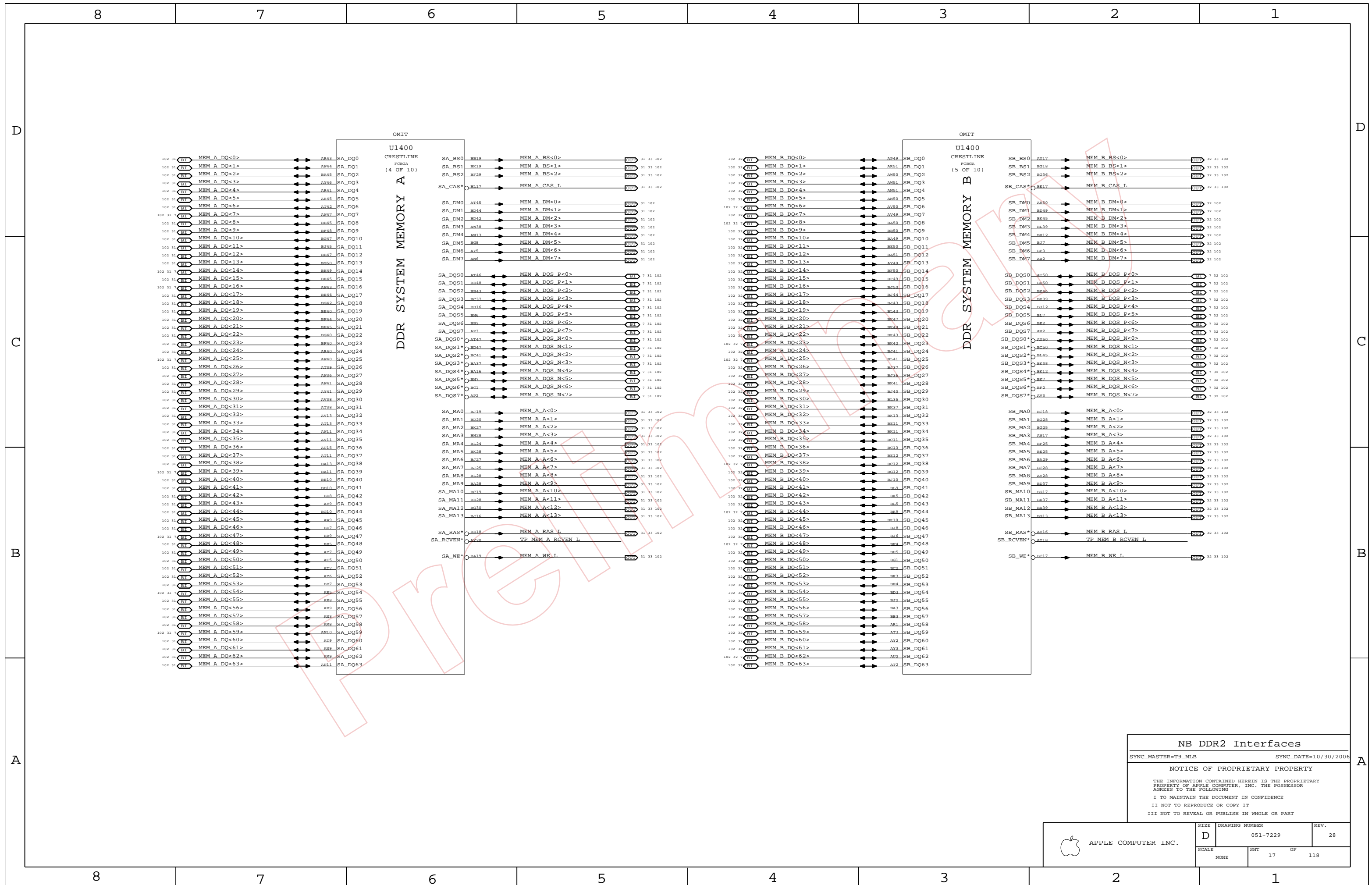
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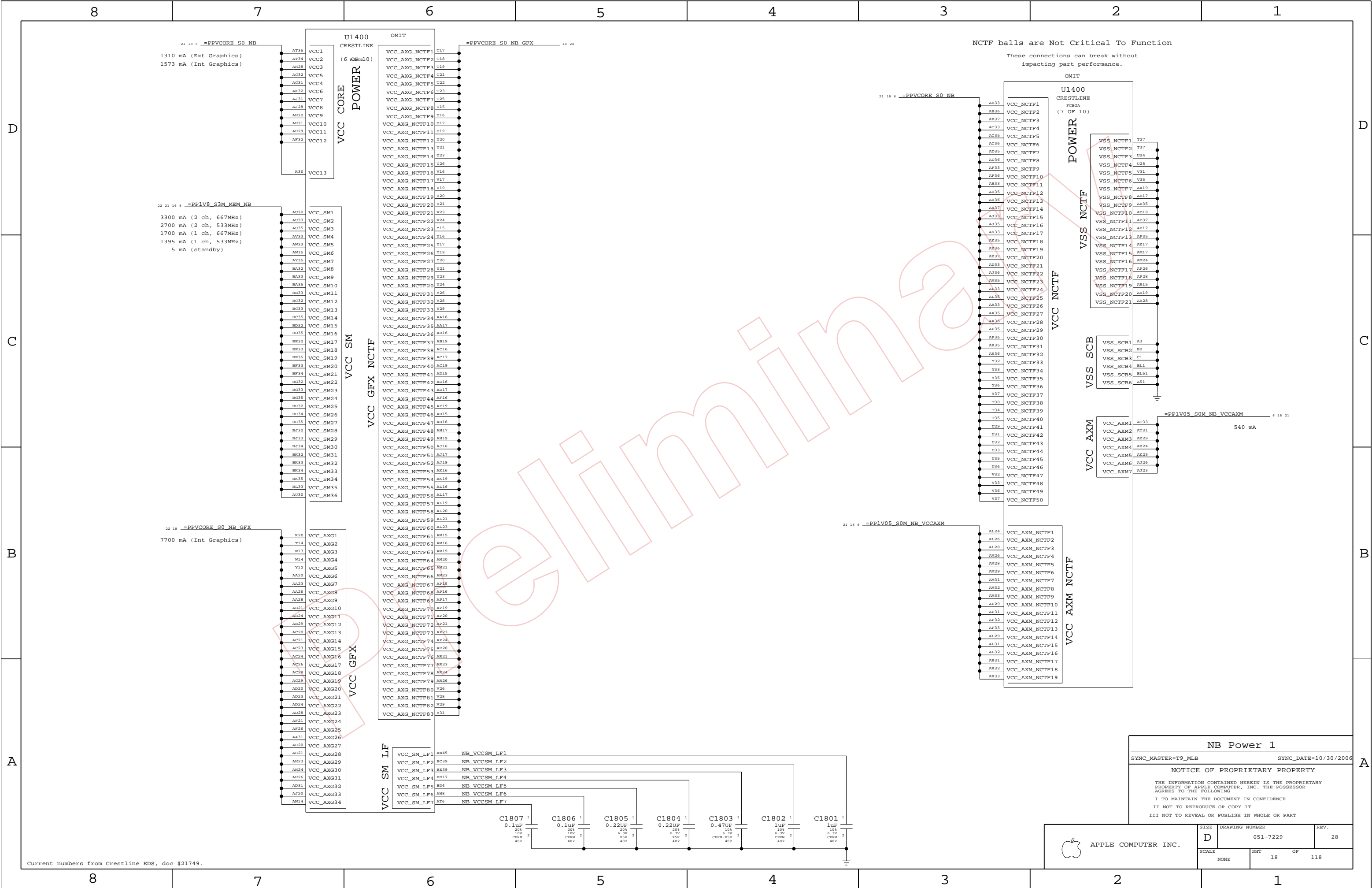
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SCALE	SHT		
	NONE	14	OF 118



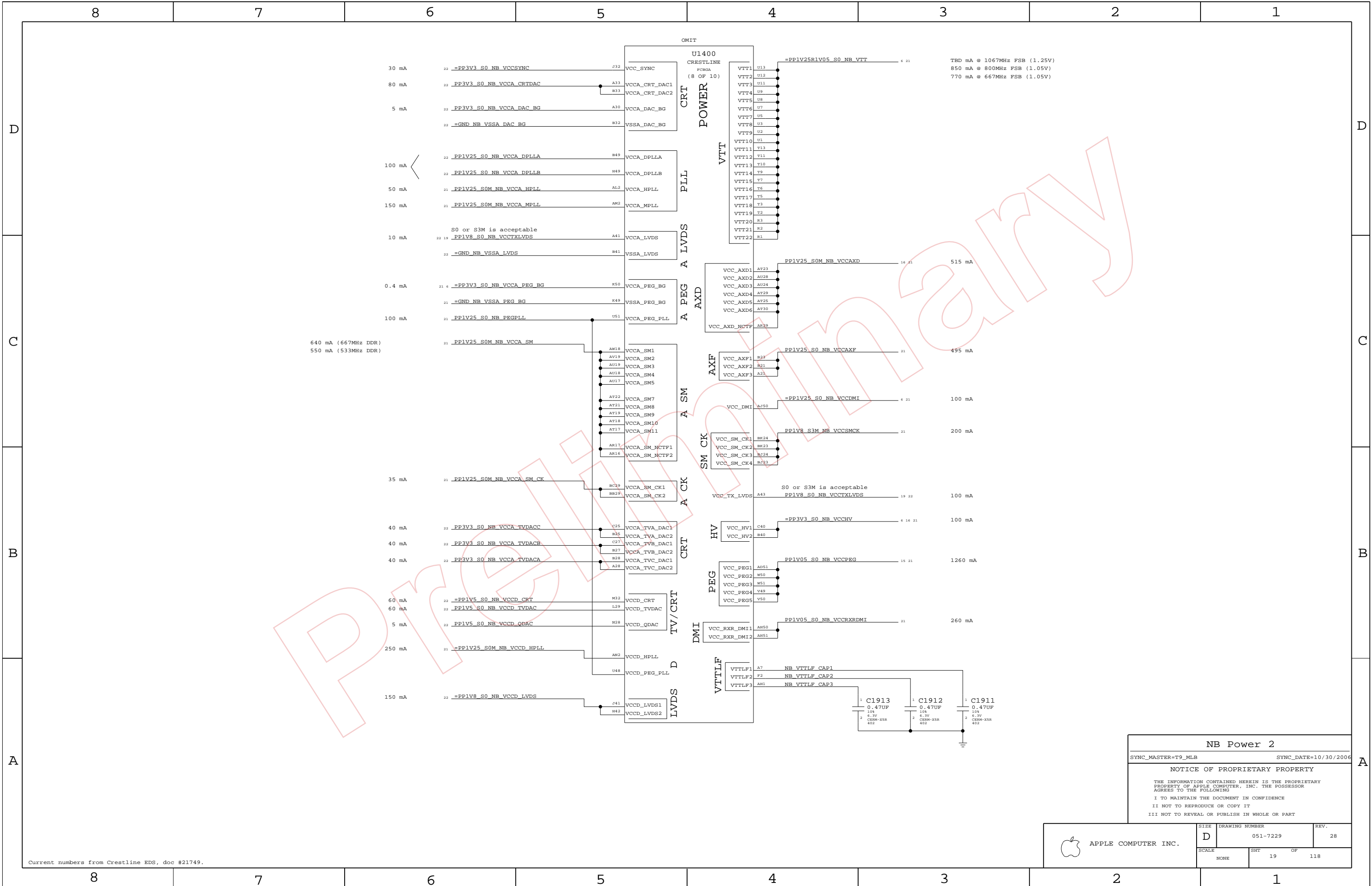






NB Power 1	
SYNC_MASTER=T9_MLB	SYNC_DATE=10/30/2006
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	SCALE NONE	SHT 18	OF 118



NB Power 2

SYNC_MASTER=T9_MLB

SYNC_DATE=10/30/2006

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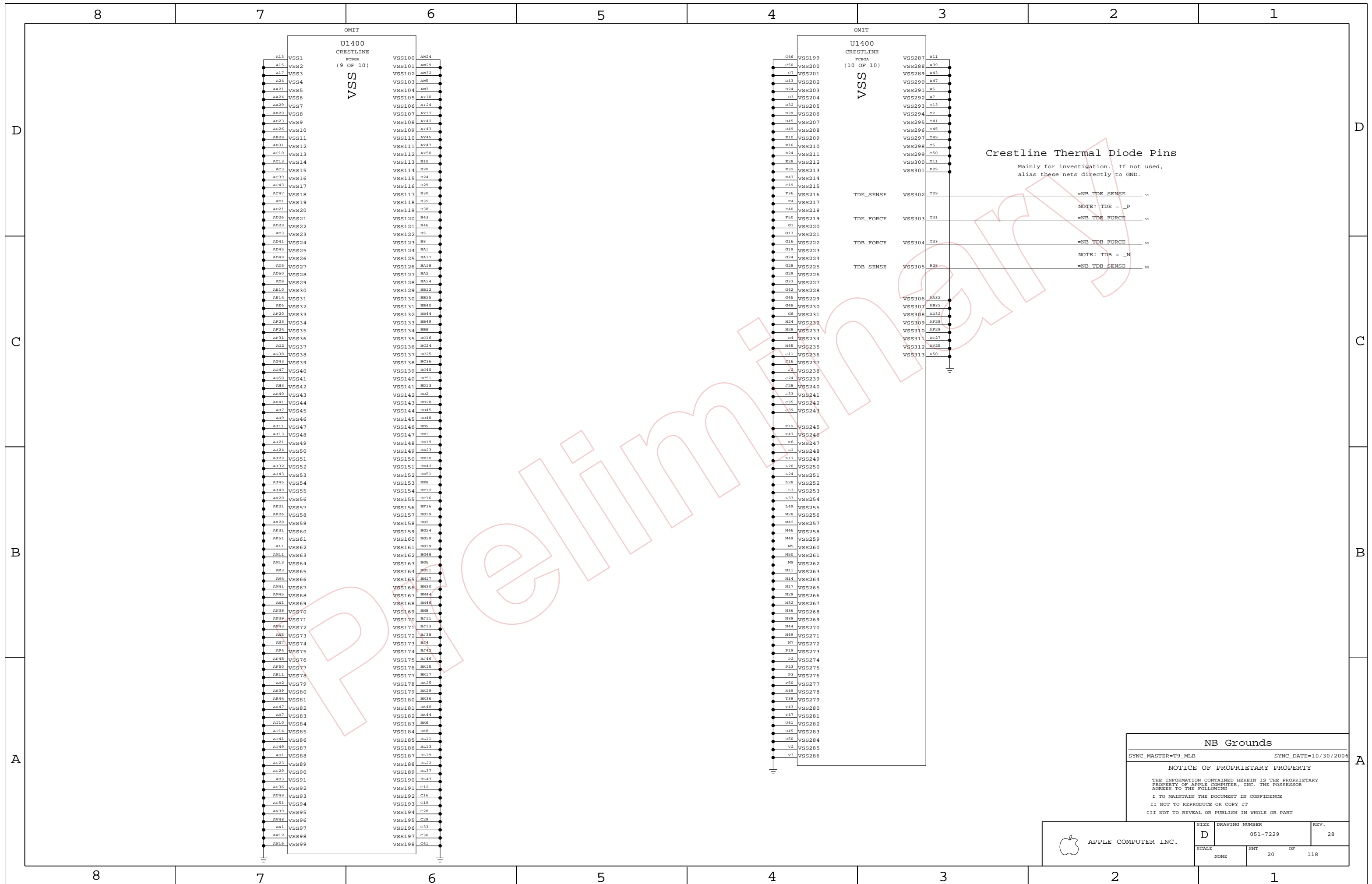
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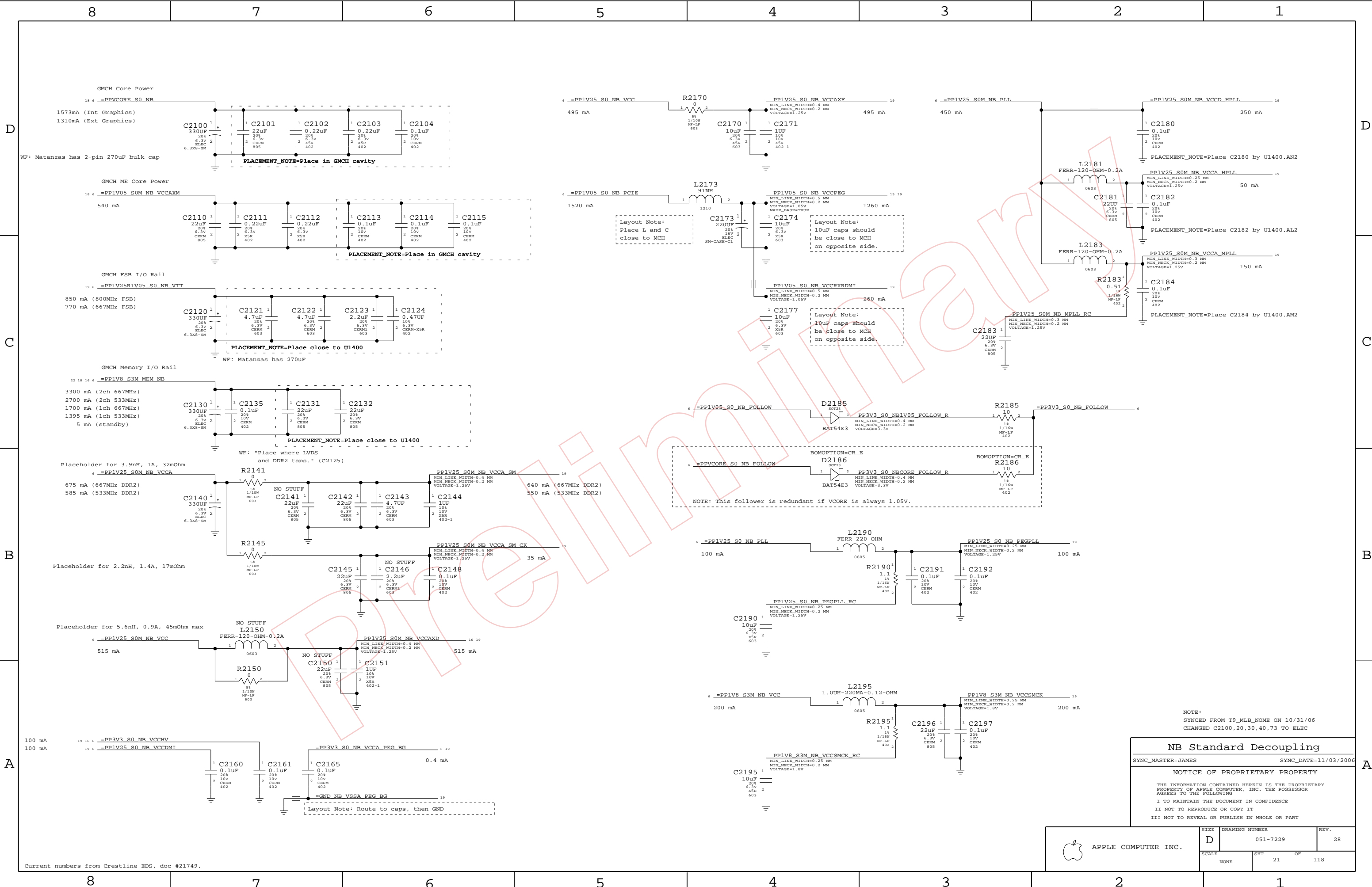
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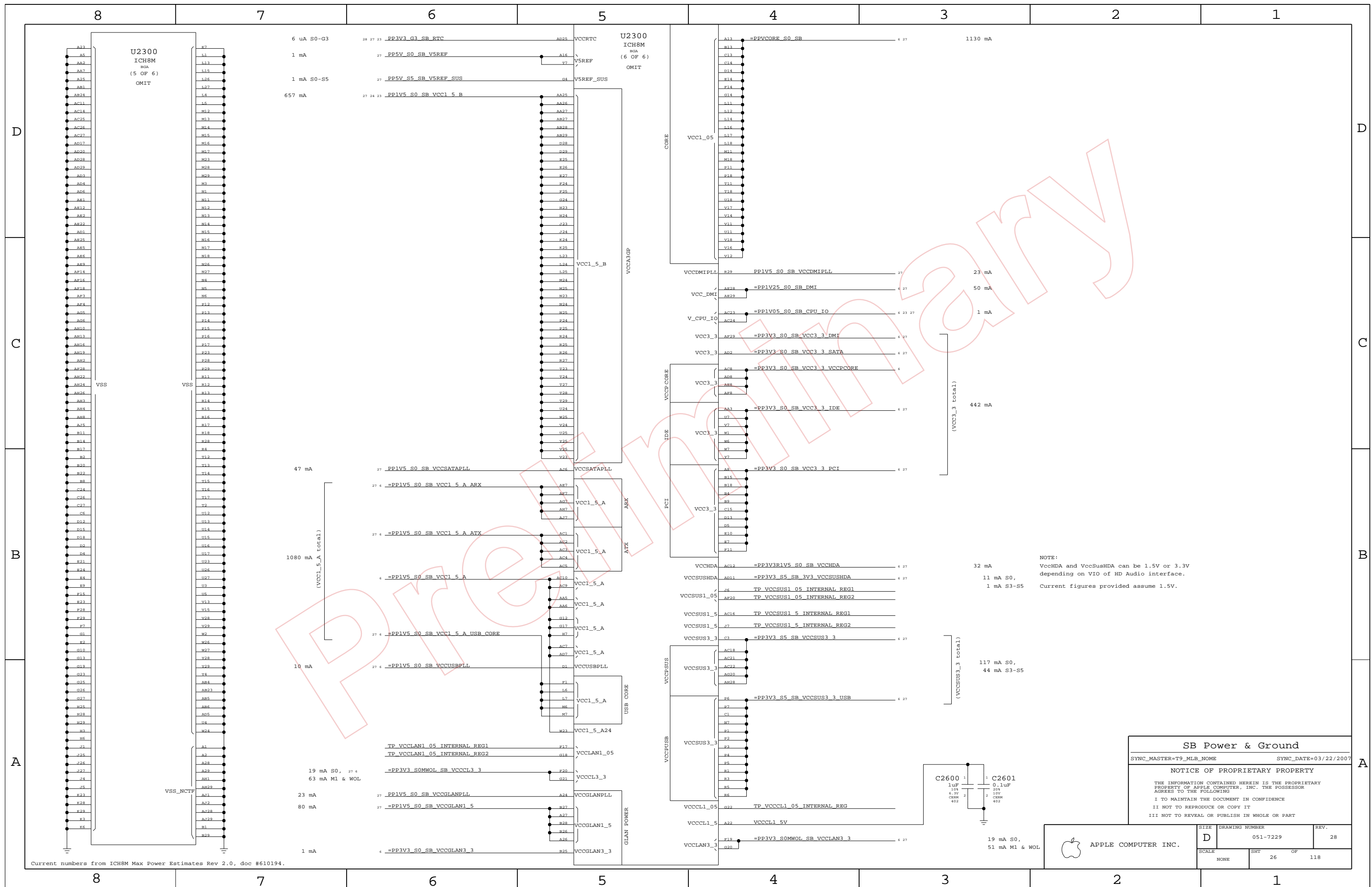


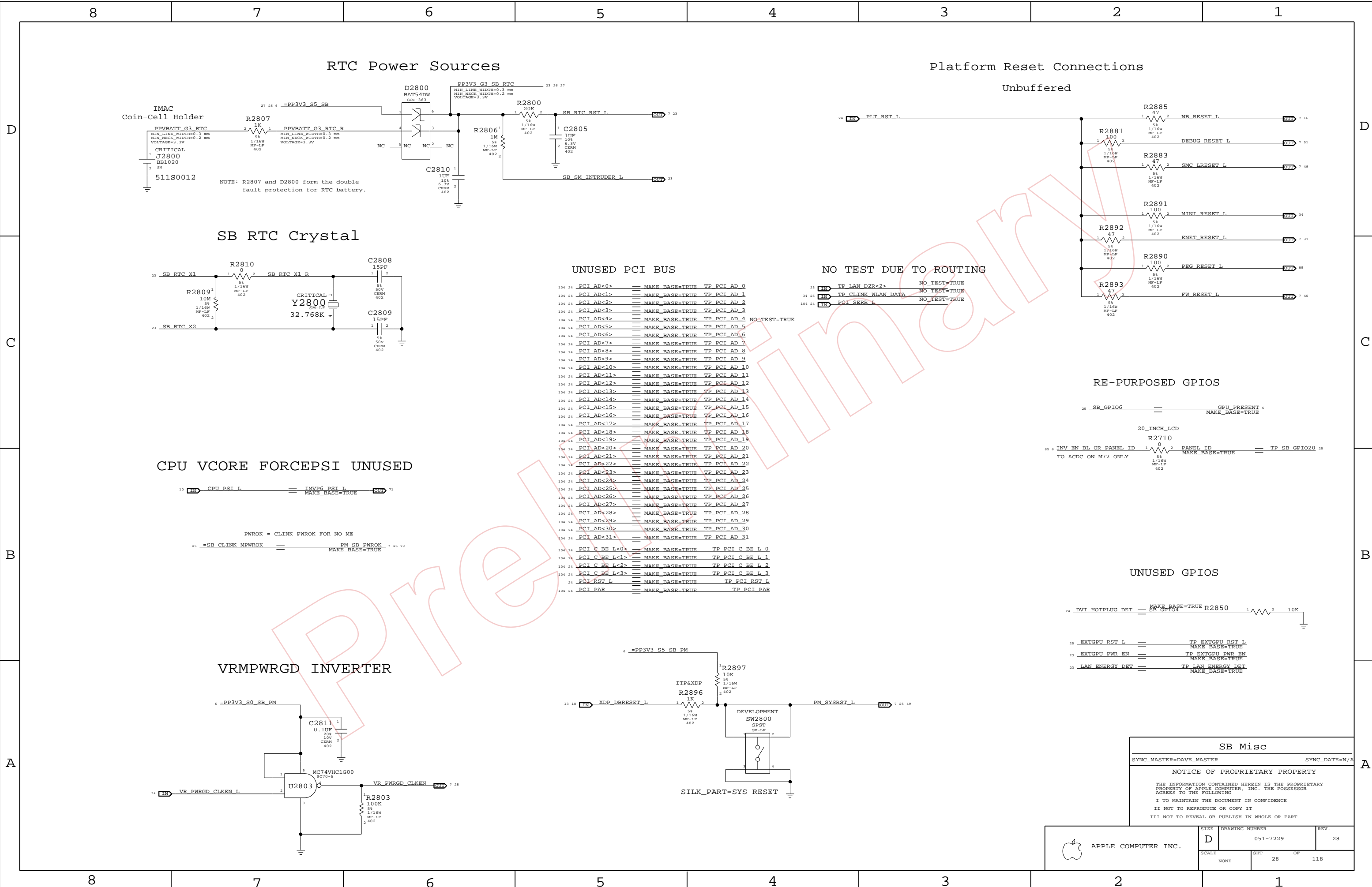


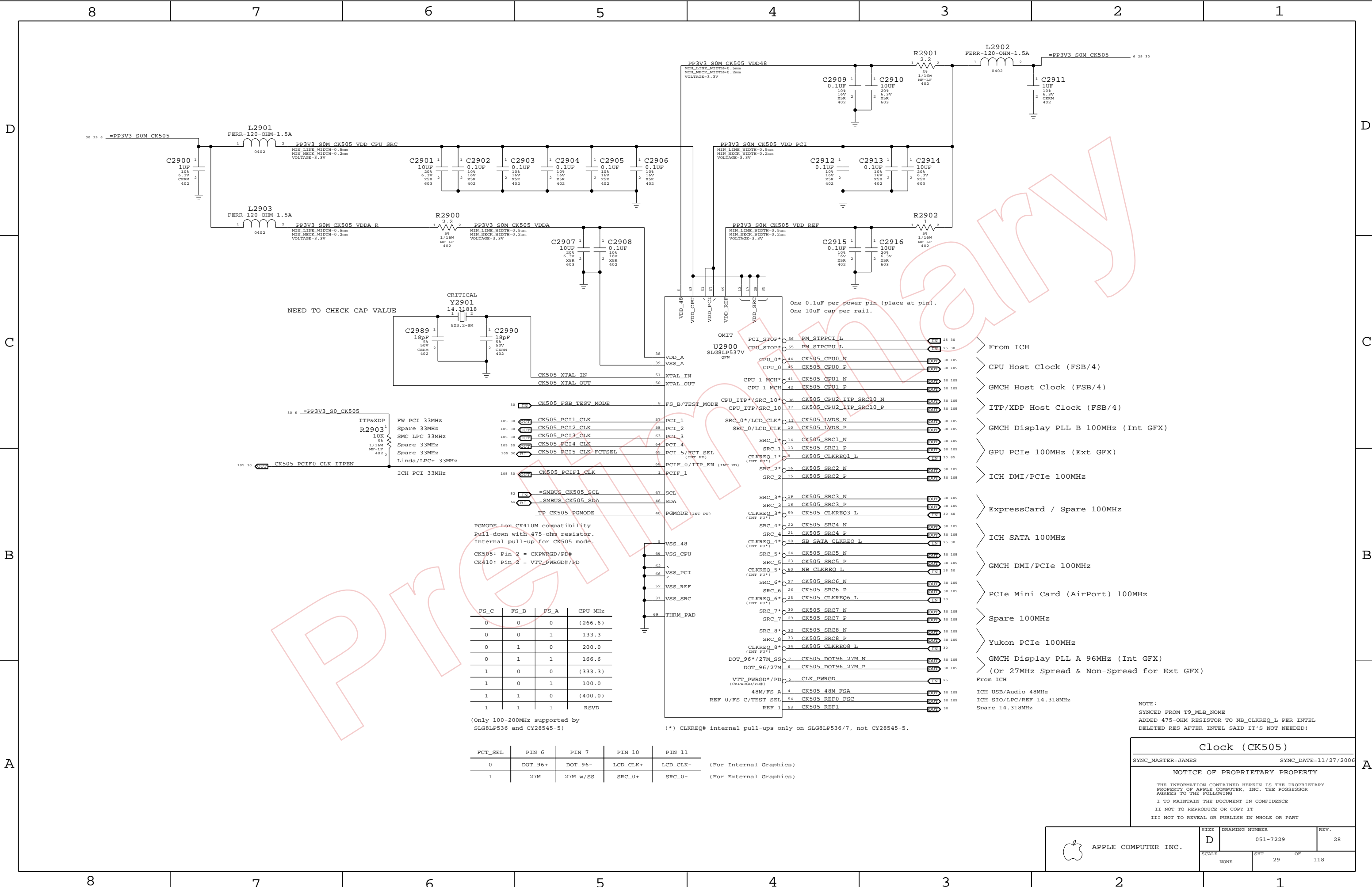
NB Standard Decoupling	
SYNC_MASTER=JAMES	SYNC_DATE=11/03/2006
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NONE		21	118

Current numbers from Crestline EDS, doc #21749.







FS_C	FS_B	FS_A	CPU MHz
0	0	0	(266.6)
0	0	1	133.3
0	1	0	200.0
0	1	1	166.6
1	0	0	(333.3)
1	0	1	100.0
1	1	0	(400.0)
1	1	1	RSVD

(Only 100-200MHz supported by
SLG8LP536 and CY28545-5)

FCT_SEL	PIN 6	PIN 7	PIN 10	PIN 11
0	DOT_96+	DOT_96-	LCD_CLK+	LCD_CLK-
1	27M	27M w/SS	SRC_0+	SRC_0-

(For Internal Graphics)
(For External Graphics)

- > From ICH
 - > CPU Host Clock (FSB/4)
 - > GMCH Host Clock (FSB/4)
 - > ITP/XDP Host Clock (FSB/4)
 - > GMCH Display PLL B 100MHz (Int GFX)
 - > GPU PCIe 100MHz (Ext GFX)
 - > ICH DMI/PCIe 100MHz
 - > ExpressCard / Spare 100MHz
 - > ICH SATA 100MHz
 - > GMCH DMI/PCIe 100MHz
 - > PCIe Mini Card (AirPort) 100MHz
 - > Spare 100MHz
 - > Yukon PCIe 100MHz
 - > GMCH Display PLL A 96MHz (Int GFX)
 - > (Or 27MHz Spread & Non-Spread for Ext GFX)
- From ICH
- ICH USB/Audio 48MHz
- ICH SIO/LPC/REF 14.318MHz
- Spare 14.318MHz

NOTE:
SYNCED FROM T9_MLB_NAME
ADDED 475-OHM RESISTOR TO NB_CLKREQ_L PER INTEL
DELETED RES AFTER INTEL SAID IT'S NOT NEEDED!

Clock (CK505)

SYNC_MASTER=JAMES SYNC_DATE=11/27/2006

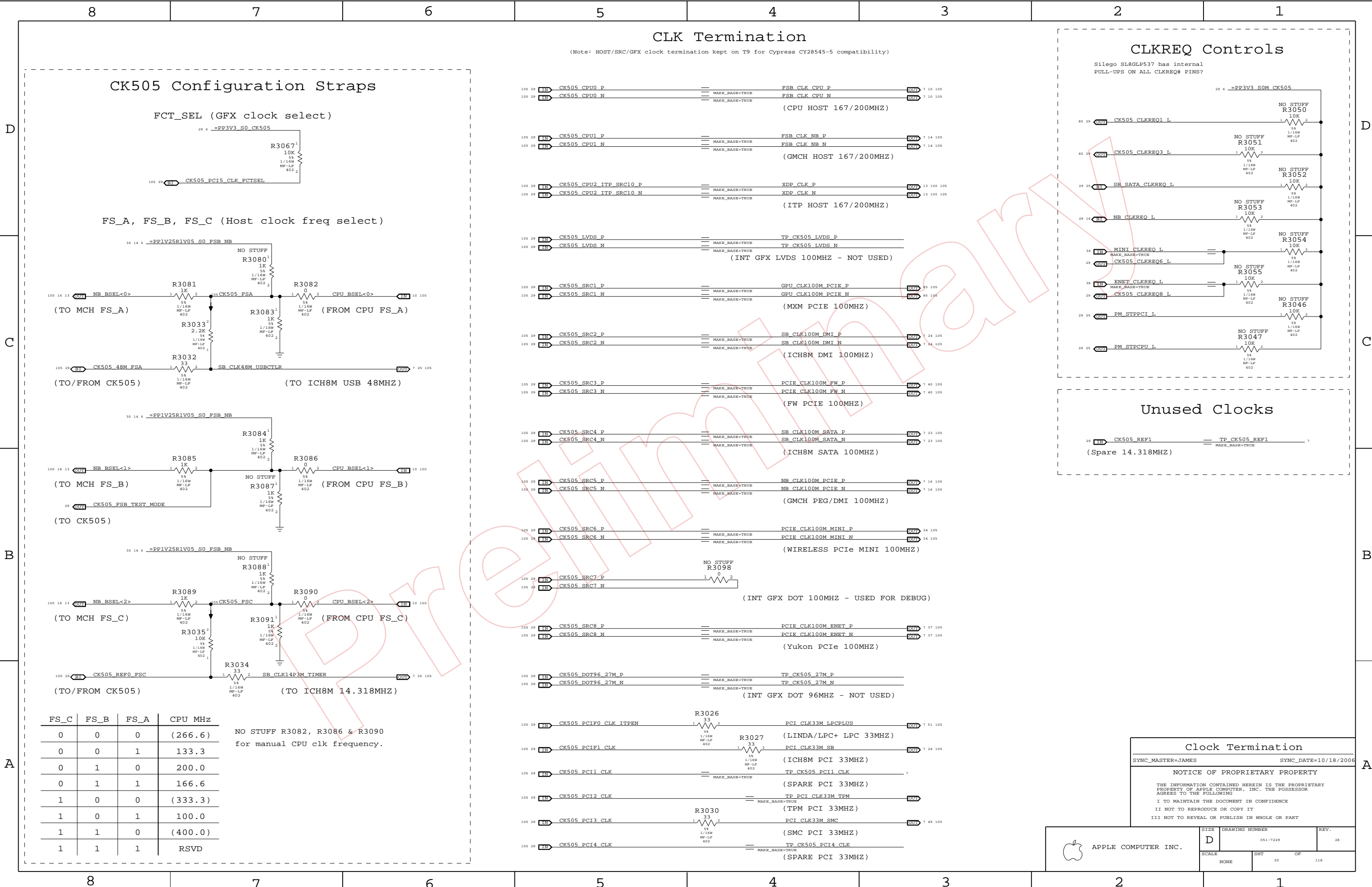
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SIZE	DRAWING NUMBER	REV.
D	051-7229	28
SCALE	SHT	OF
NONE	29	118



Page Notes

Power aliases required by this page:

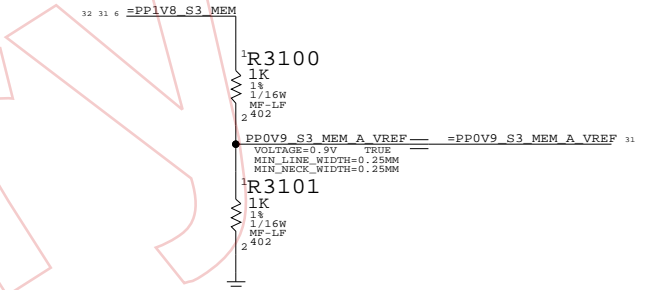
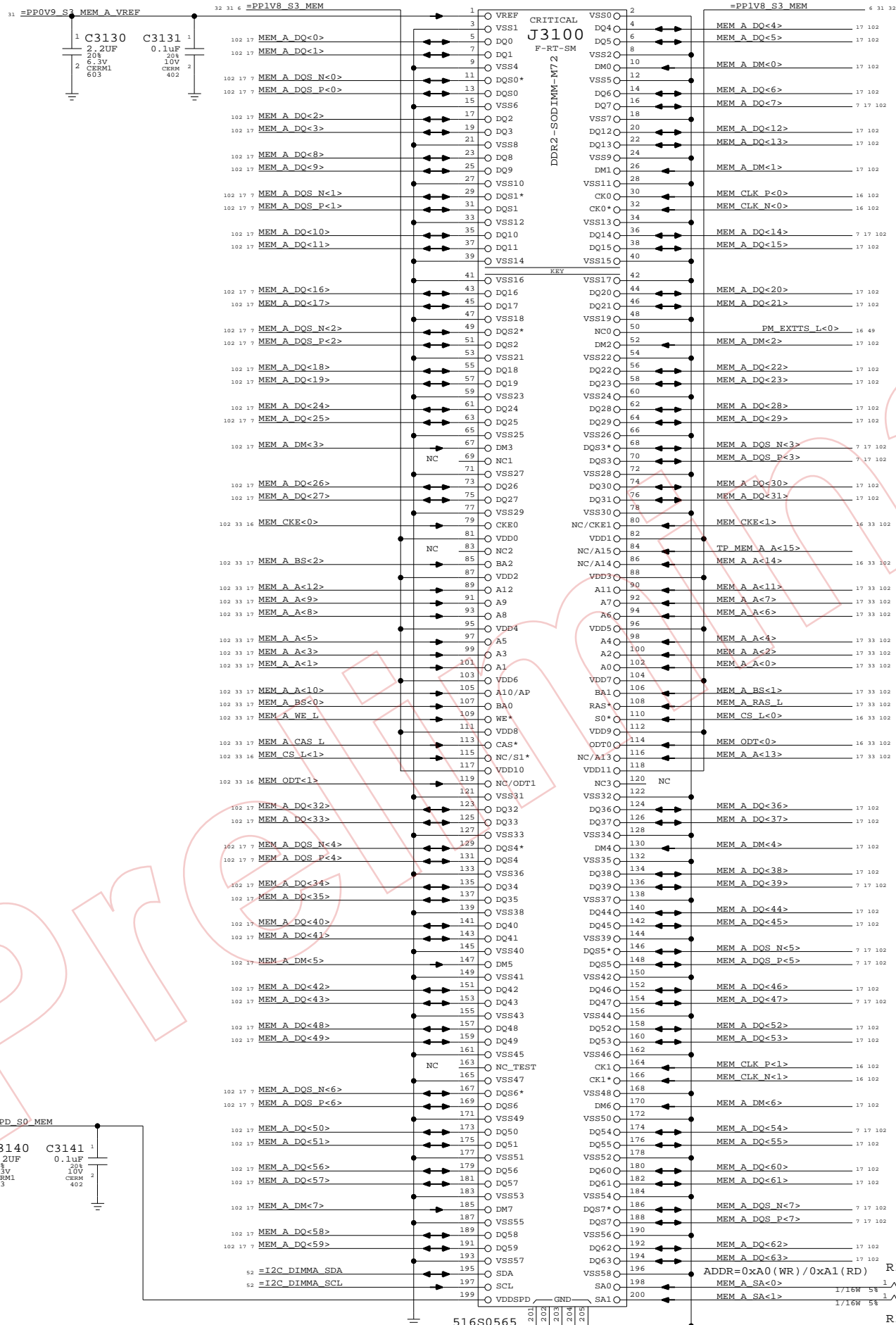
```
- =PP1V8_S3_MEM
- =PP0V9_S3_MEM_VREF
- =PPSPD_S0_MEM (2.5V - 3.3V)
```

Signal aliases required by this page:

- =I2C_MEM_SCL
- =I2C_MEM_SDA

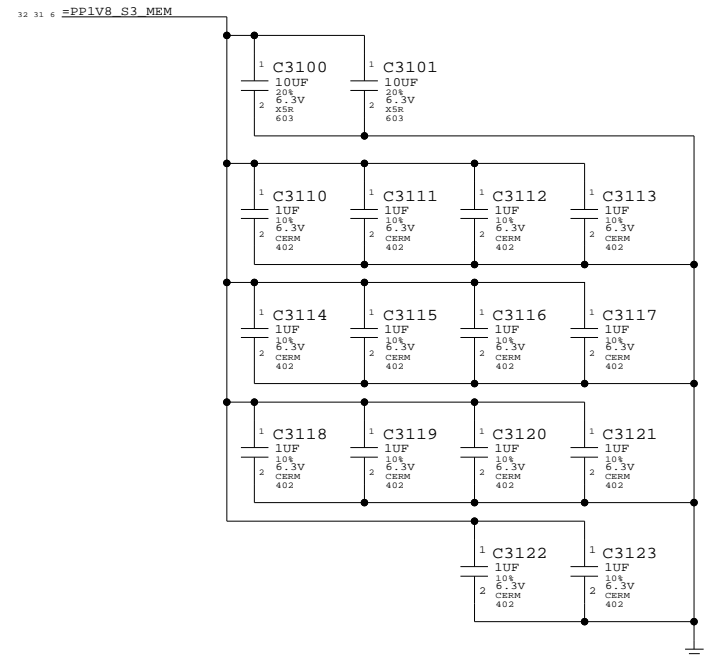
BOM options provided by this page:
(NONE)

NOTE: This page does not supply VREF.
The reference voltage must be provided
by another page.



DDR2 Bypass Caps

(For return current)



DDR2 SO-DIMM Connector A

SYNC_MASTER=JAMES	SYNC_DATE=10/17/06
-------------------	--------------------

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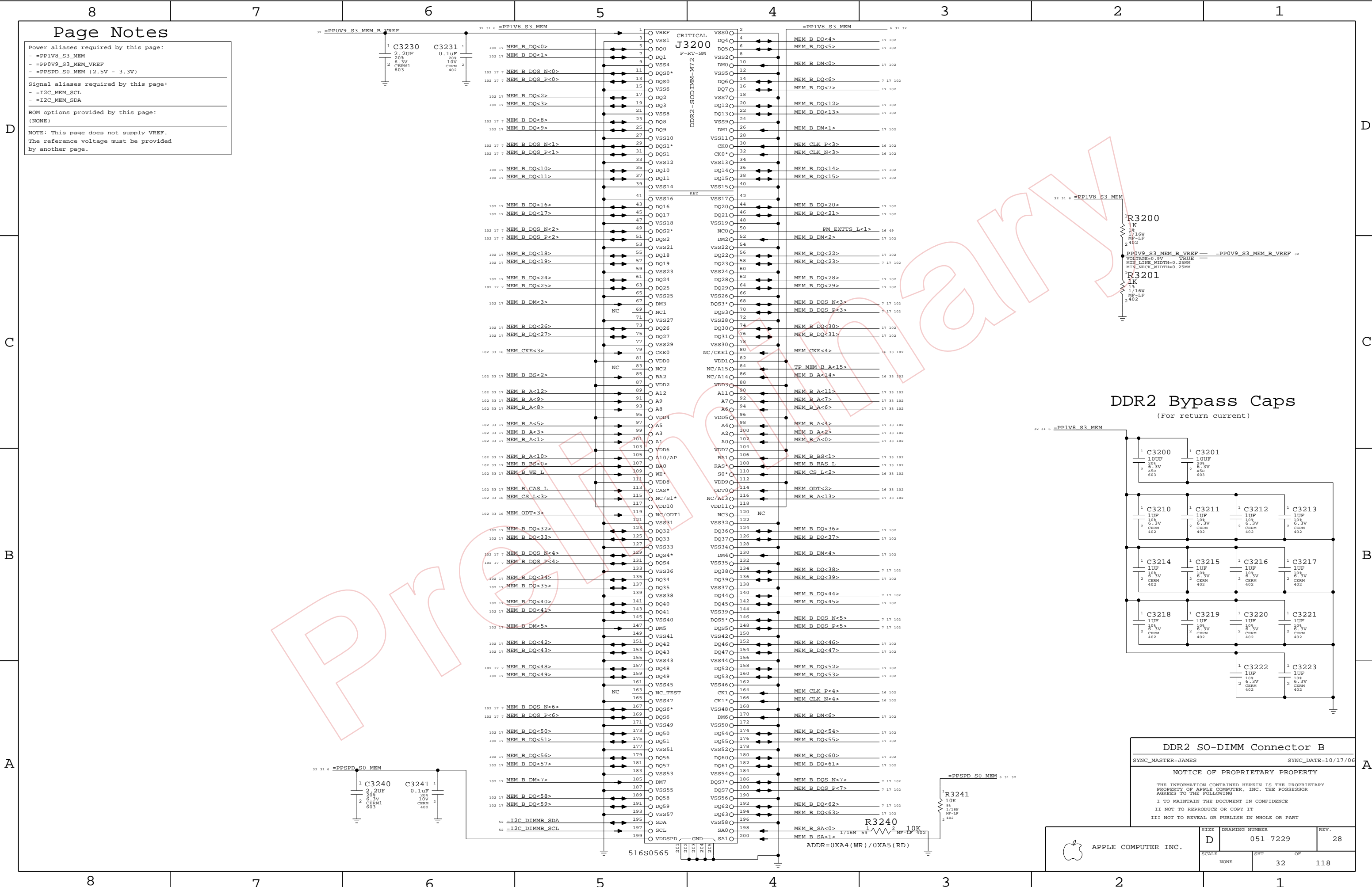
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
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D	051-7229	28
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DATE	SUBJECT	

SCALE	SH1	OF
NONE	31	118



Page Notes

Power aliases required by this page:

- =PP1V8_S3_MEM

- =PP0V9_S3_MEM_VREF

- =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:

- =I2C_MEM_SCL

- =I2C_MEM_SDA

BOM options provided by this page:

(NONE)

NOTE: This page does not supply VREF.

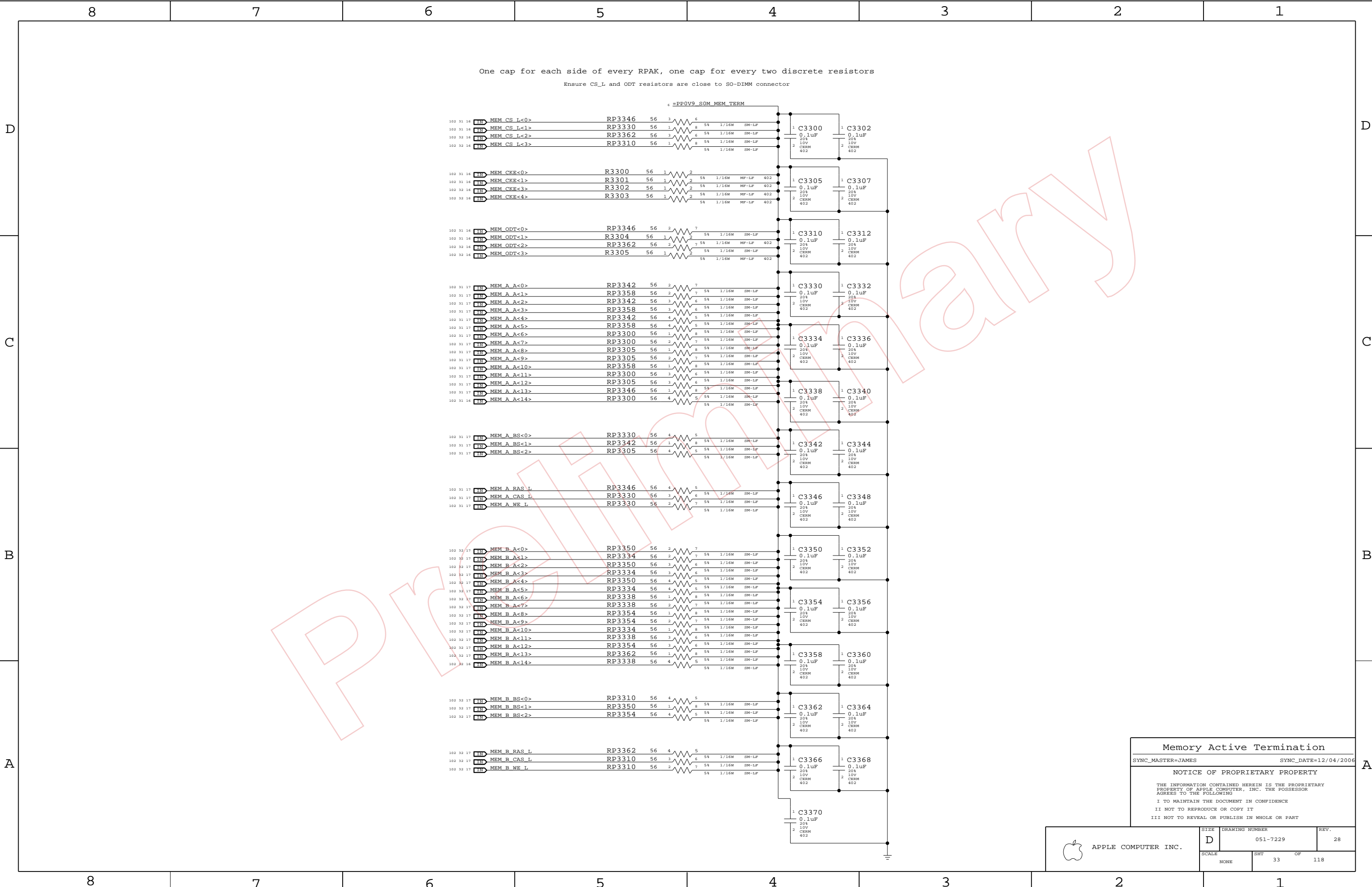
The reference voltage must be provided by another page.

DDR2 Bypass Caps

(For return current)

DDR2 SO-DIMM Connector B		
SYNC_MASTER=JAMES		SYNC_DATE=10/17/06
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	D	051-7229	28
SCALE		SHT	OF
NONE		32	118



Memory Active Termination

SYNC_MASTER=JAMES SYNC_DATE=12/04/2006

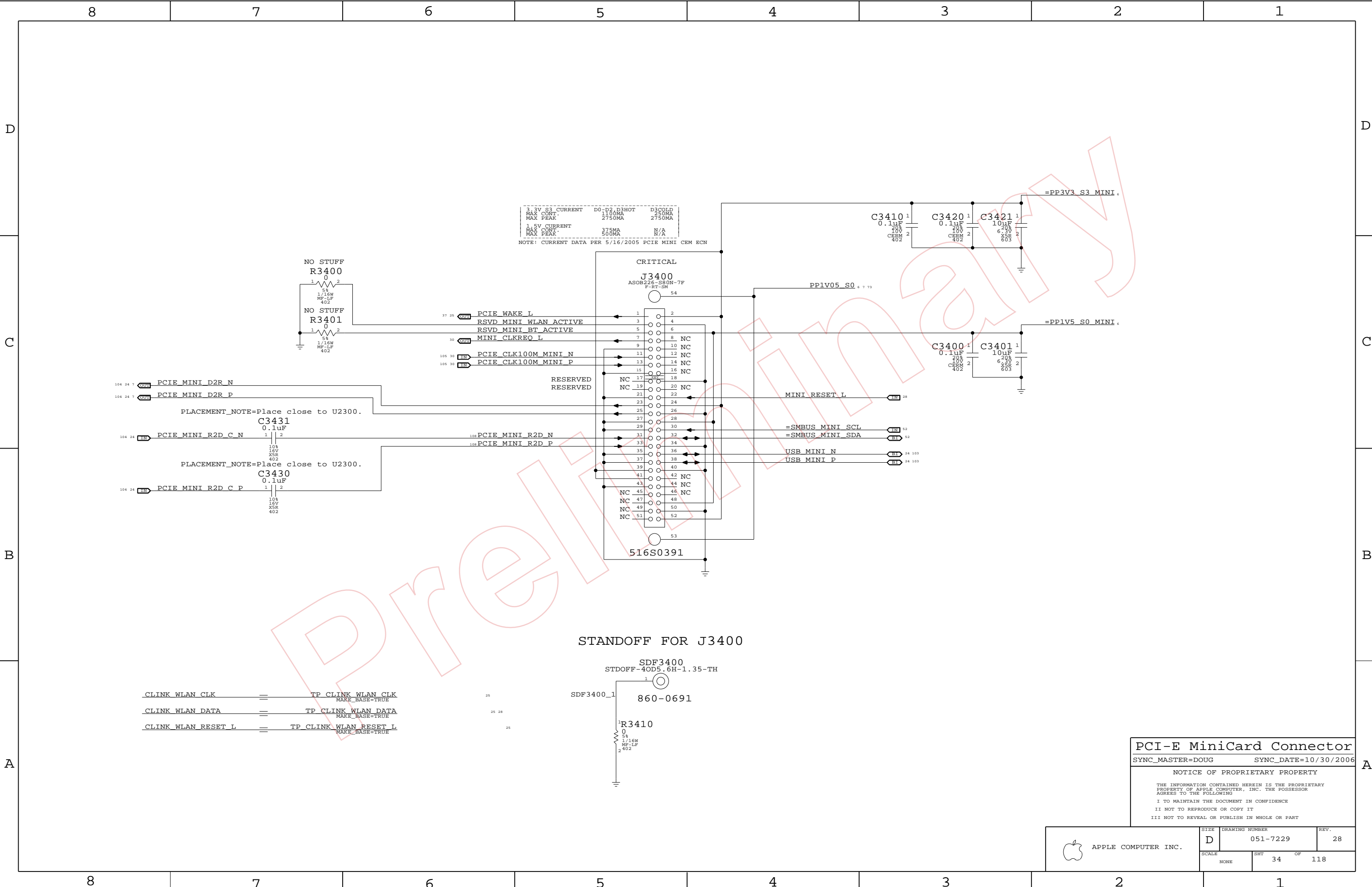
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PCI-E MiniCard Connector

SYNC_MASTER=DOUG SYNC_DATE=10/30/2006

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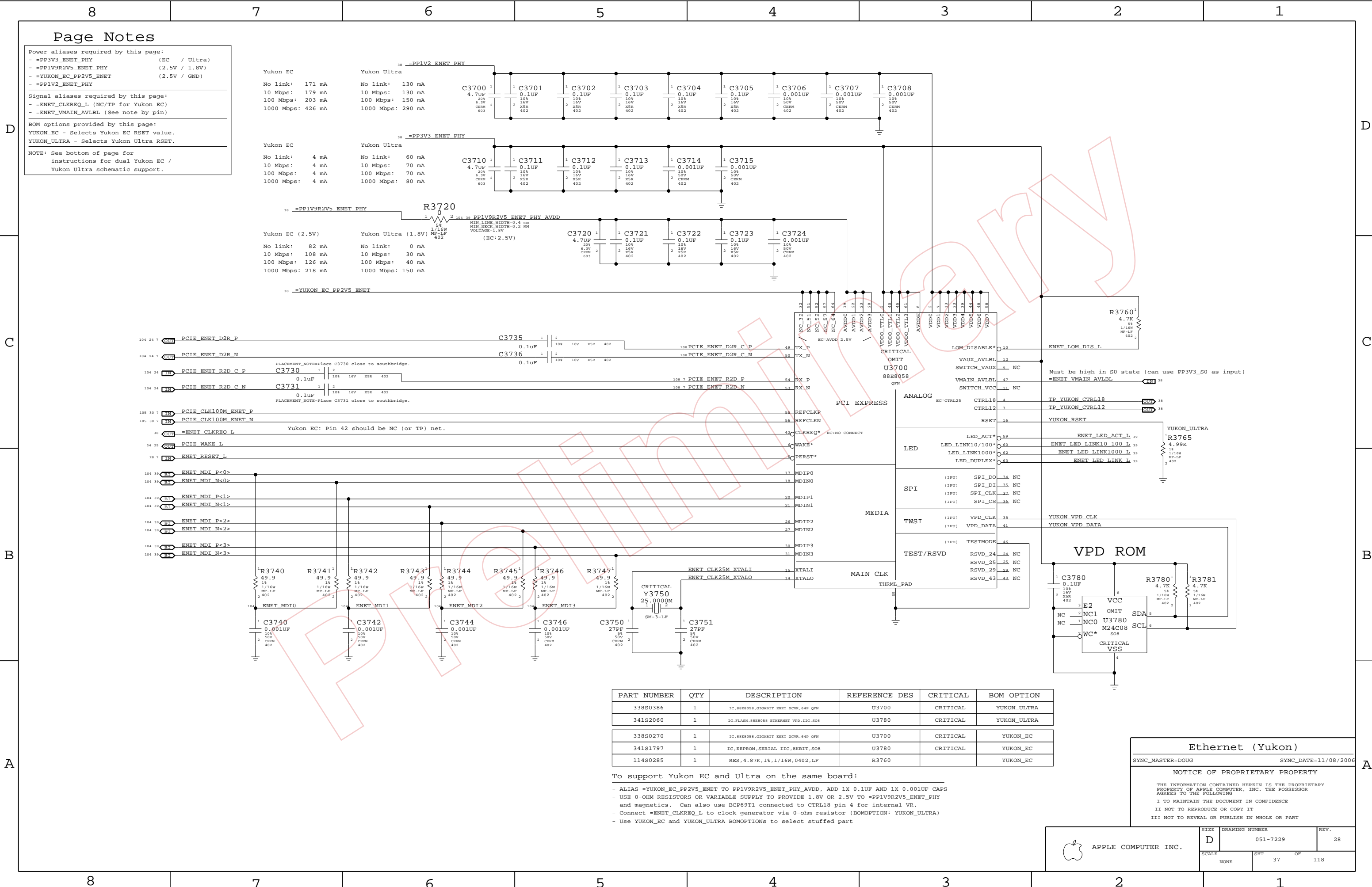
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APPLE COMPUTER INC.

SIZE D DRAWING NUMBER 051-7229 REV. 28

SCALE NONE SHT 34 OF 118



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S0386	1	IC,88E8058,GIGABIT ENET XCVR,64P QFN	U3700	CRITICAL	YUKON_ULTRA
341S2060	1	IC,FLASH,88E8058 ETHERNET VPD,IIC,S08	U3780	CRITICAL	YUKON_ULTRA
338S0270	1	IC,88E8058,GIGABIT ENET XCVR,64P QFN	U3700	CRITICAL	YUKON_EC
341S1797	1	IC,EEPROM,SERIAL IIC,8KBIT,S08	U3780	CRITICAL	YUKON_EC
114S0285	1	RES,4.87K,1%,1/16W,0402,LF	R3760		YUKON_EC

To support Yukon EC and Ultra on the same board:

- ALIAS =YUKON_EC_PP2V5_ENET TO PP1V9R2V5_ENET_PHY_AVDD, ADD 1X 0.1uF AND 1X 0.001uF CAPS
- USE 0-OHM RESISTORS OR VARIABLE SUPPLY TO PROVIDE 1.8V OR 2.5V TO =PP1V9R2V5_ENET_PHY and magnetics. Can also use BCP69T1 connected to CTRL18 pin 4 for internal VR.
- Connect =ENET_CLKREQ_L to clock generator via 0-ohm resistor (BOMOPTION: YUKON_ULTRA)
- Use YUKON_EC and YUKON_ULTRA BOMOPTIONS to select stuffed part

Ethernet (Yukon)

SYNC_MASTER=DOUG SYNC_DATE=11/08/2006

NOTICE OF PROPRIETARY PROPERTY

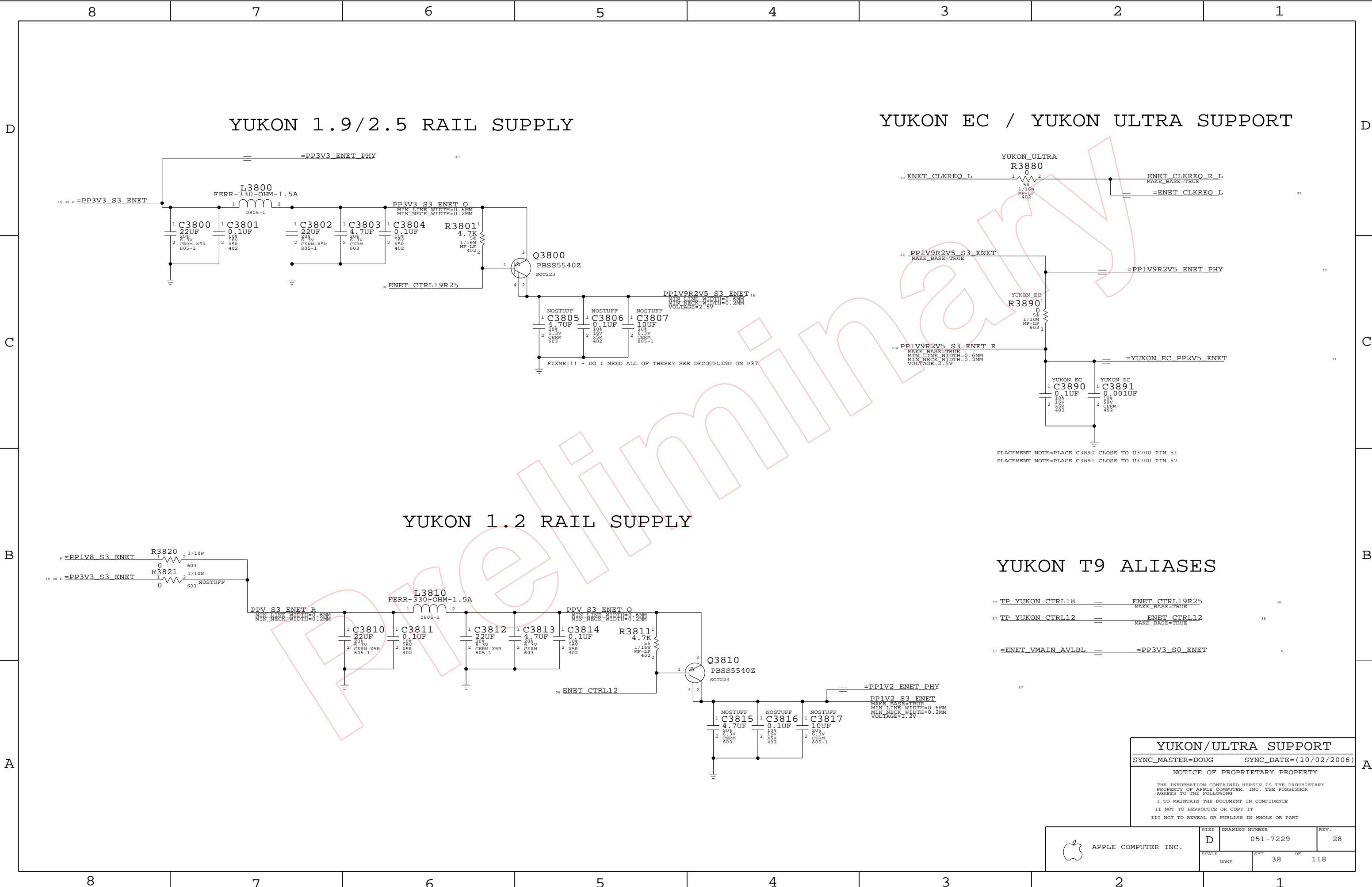
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7229	REV. 28
	SCALE NONE	SHT 37	OF 118



YUKON T9 ALIASES

37 TP_YUKON_CTRL18 = ENET_CTRL19R25 38
37 TP_YUKON_CTRL12 = ENET_CTRL12 38
37 =ENET_VMAIN_AVLBL = =PP3V3_S0_ENET 6

YUKON/ULTRA SUPPORT

SYNC_MASTER=DOUG SYNC_DATE=(10/02/2006)

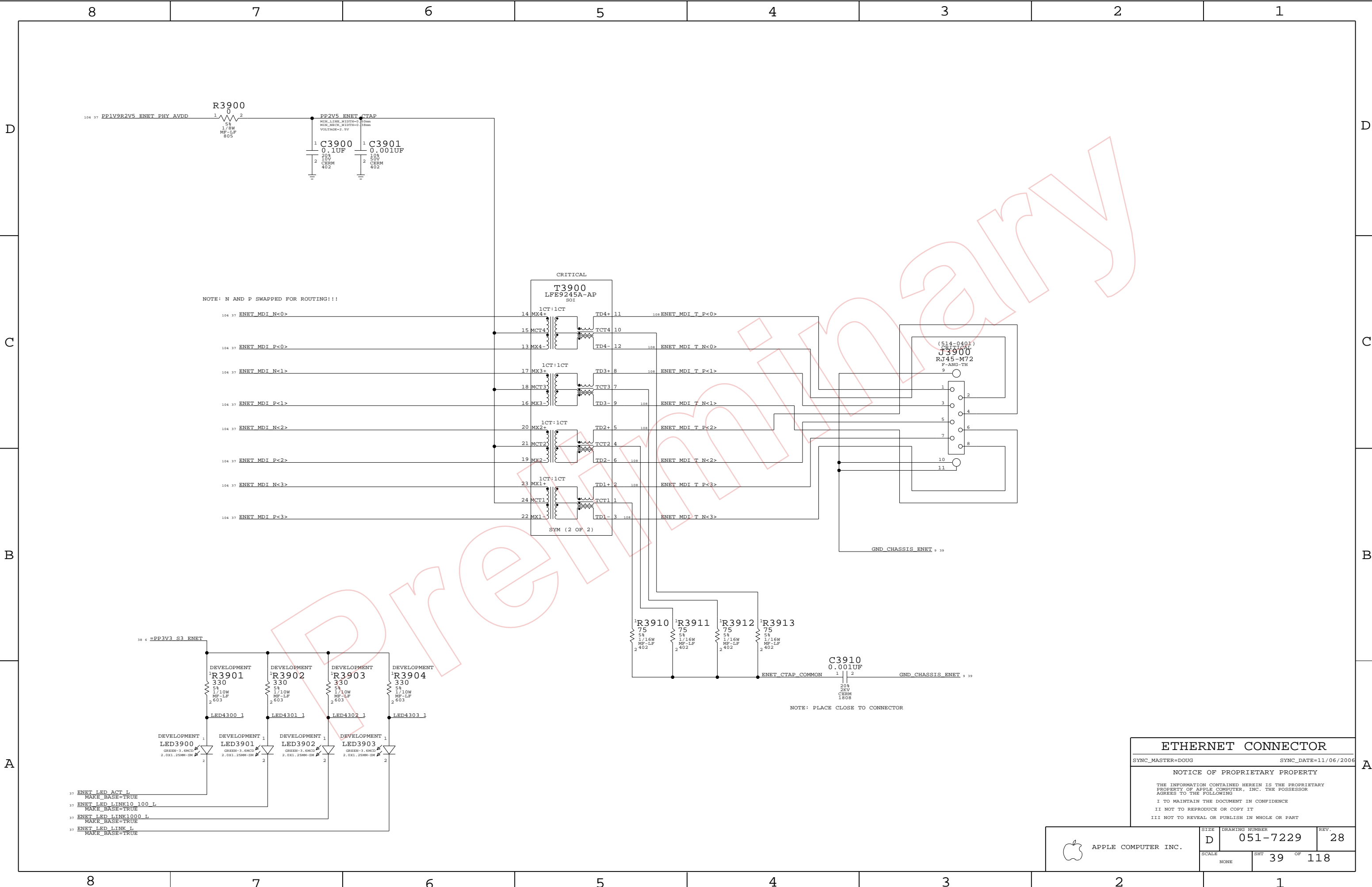
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D	051-7229	28
SCALE	SHT	OF
NONE	38	118



ETHERNET CONNECTOR

SYNC_MASTER=DOUG

SYNC_DATE=11/06/2006

NOTICE OF PROPRIETARY PROPERTY

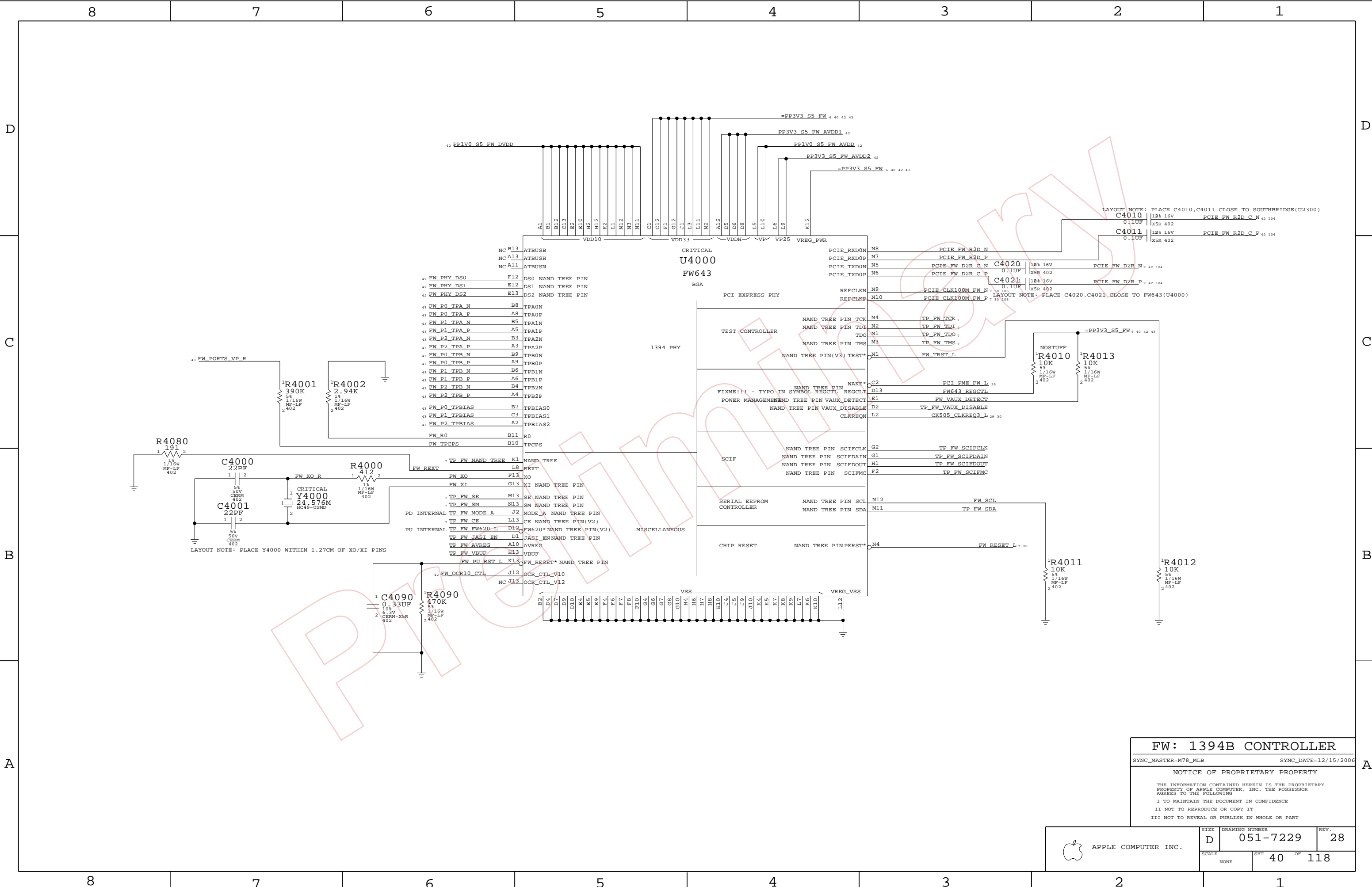
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SCALE		SHT	OF
NONE		39	118



FW: 1394B CONTROLLER

SYNC_MASTER=M78_MLB

SYNC_DATE=12/15/2006


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APPLE COMPUTER INC.

SIZE

D

DRAWING NUMBER

051-7229

REV.

28

SCALE

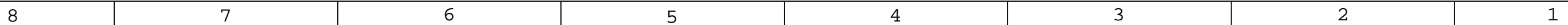
NONE

SHT

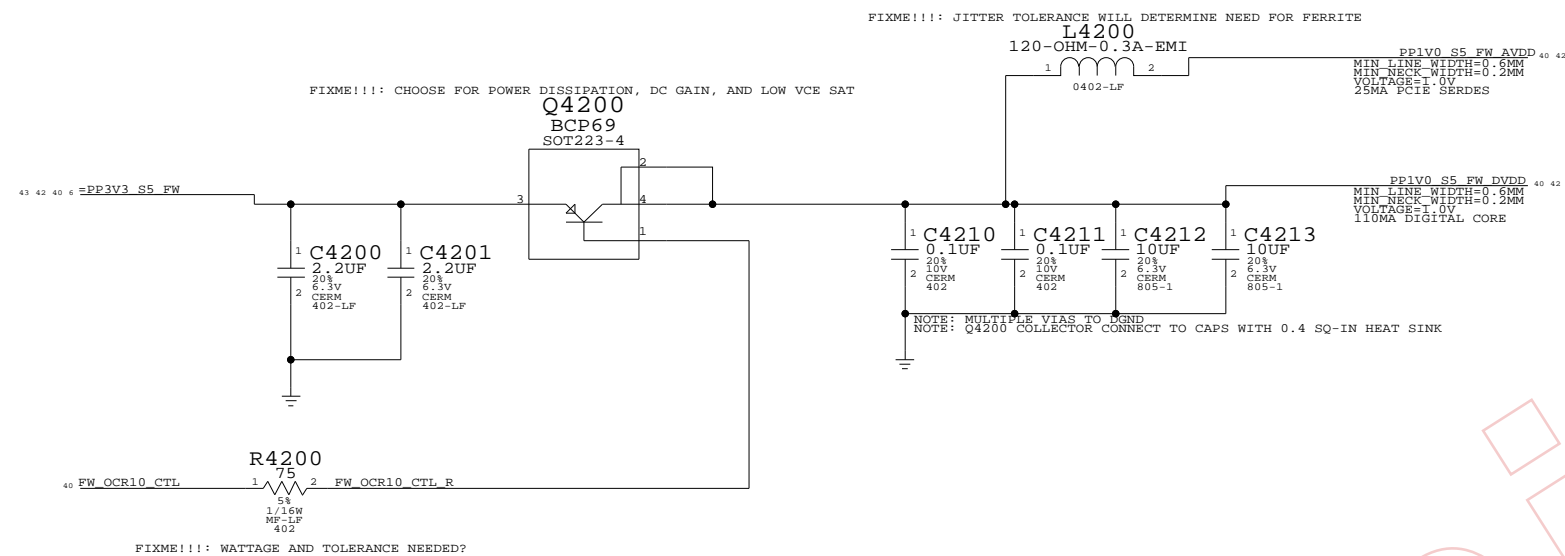
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OF

118

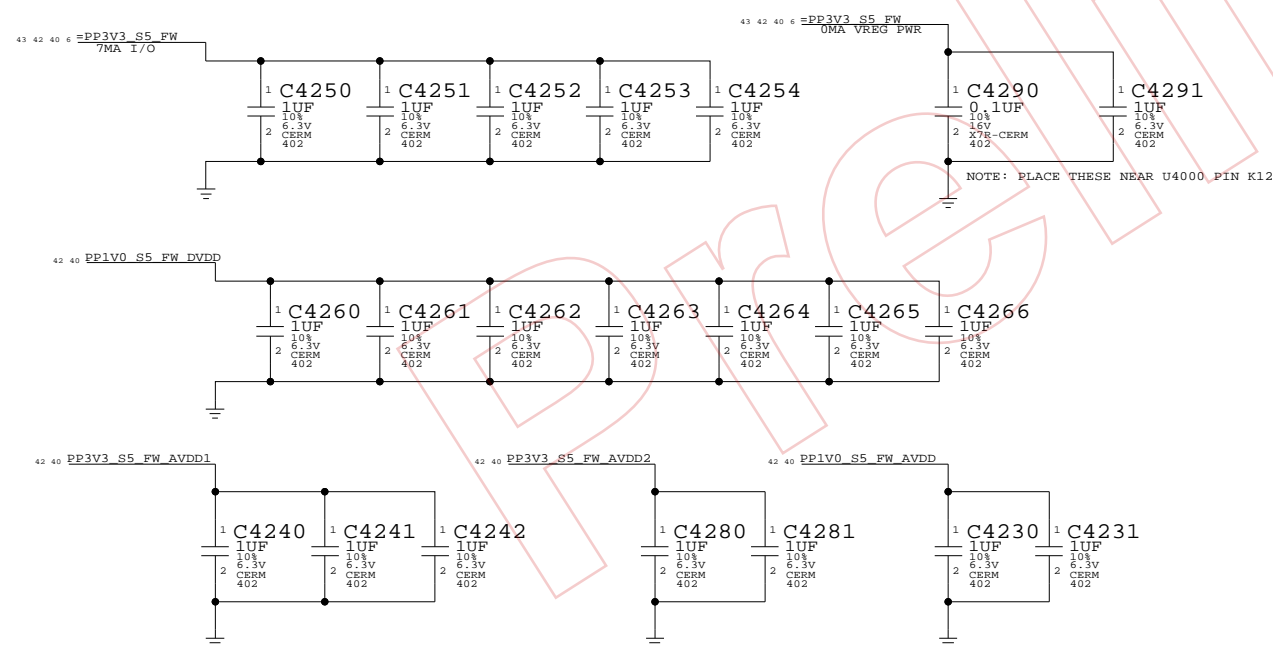


FW643 1.0V GENERATION

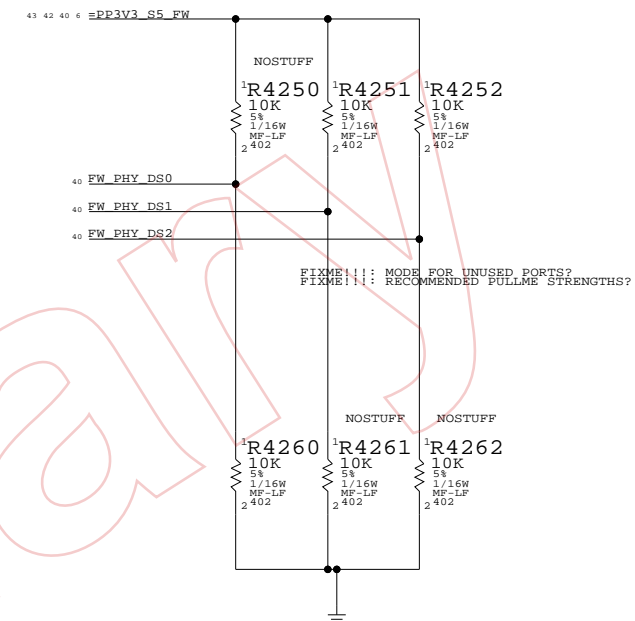


FW643 DECOUPLING

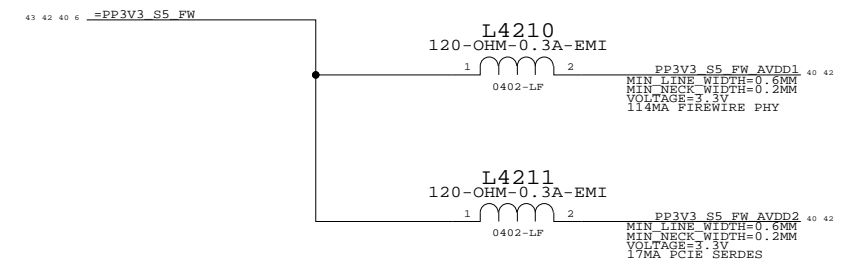
NOTE: PLACE 1 CAP CLOSE TO EACH POWER PIN ON U4000



1394 PHY DATA/STROBE OPTIONS



FW 3.3V FILTERING



FW PCIE ALIASES

24	<u>TP_PCIE_FW_R2D_C_N</u>	<u>==</u>	<u>PCIE_FW_R2D_C_N</u>	40	104
			MAKE_BASE=TRUE		
24	<u>TP_PCIE_FW_R2D_C_P</u>	<u>==</u>	<u>PCIE_FW_R2D_C_P</u>	40	104
			MAKE_BASE=TRUE		
104	<u>PCIE_FW_D2R_N</u>	<u>==</u>	<u>TP_PCIE_FW_D2R_N</u>	24	
	MAKE_BASE=TRUE				
104	<u>PCIE_FW_D2R_P</u>	<u>==</u>	<u>TP_PCIE_FW_D2R_P</u>	24	
	MAKE_BASE=TRUE				

FW: 1394B MISC

SYNC_MASTER=DOUG	SYNC_DATE=10/10/2006
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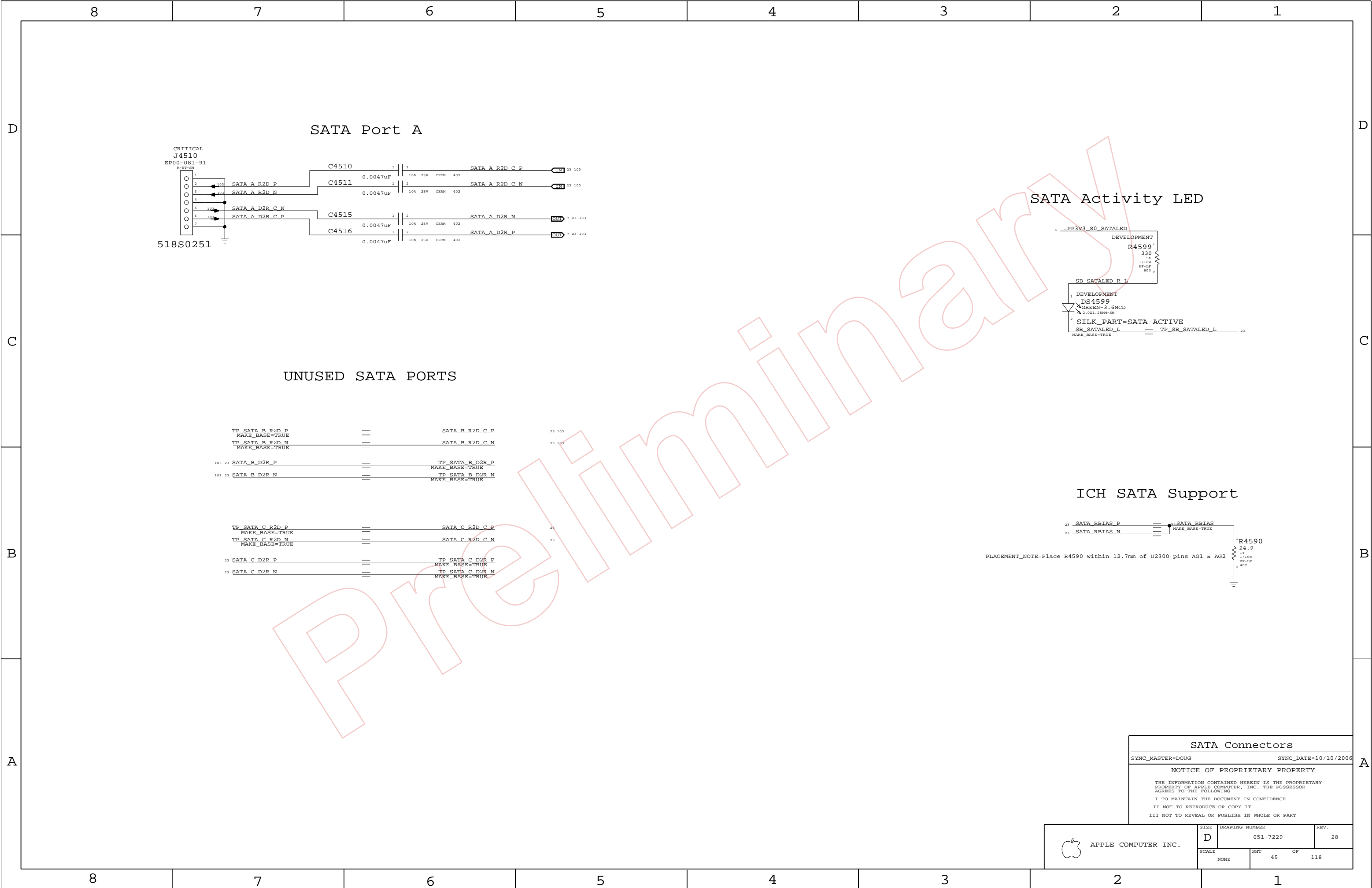
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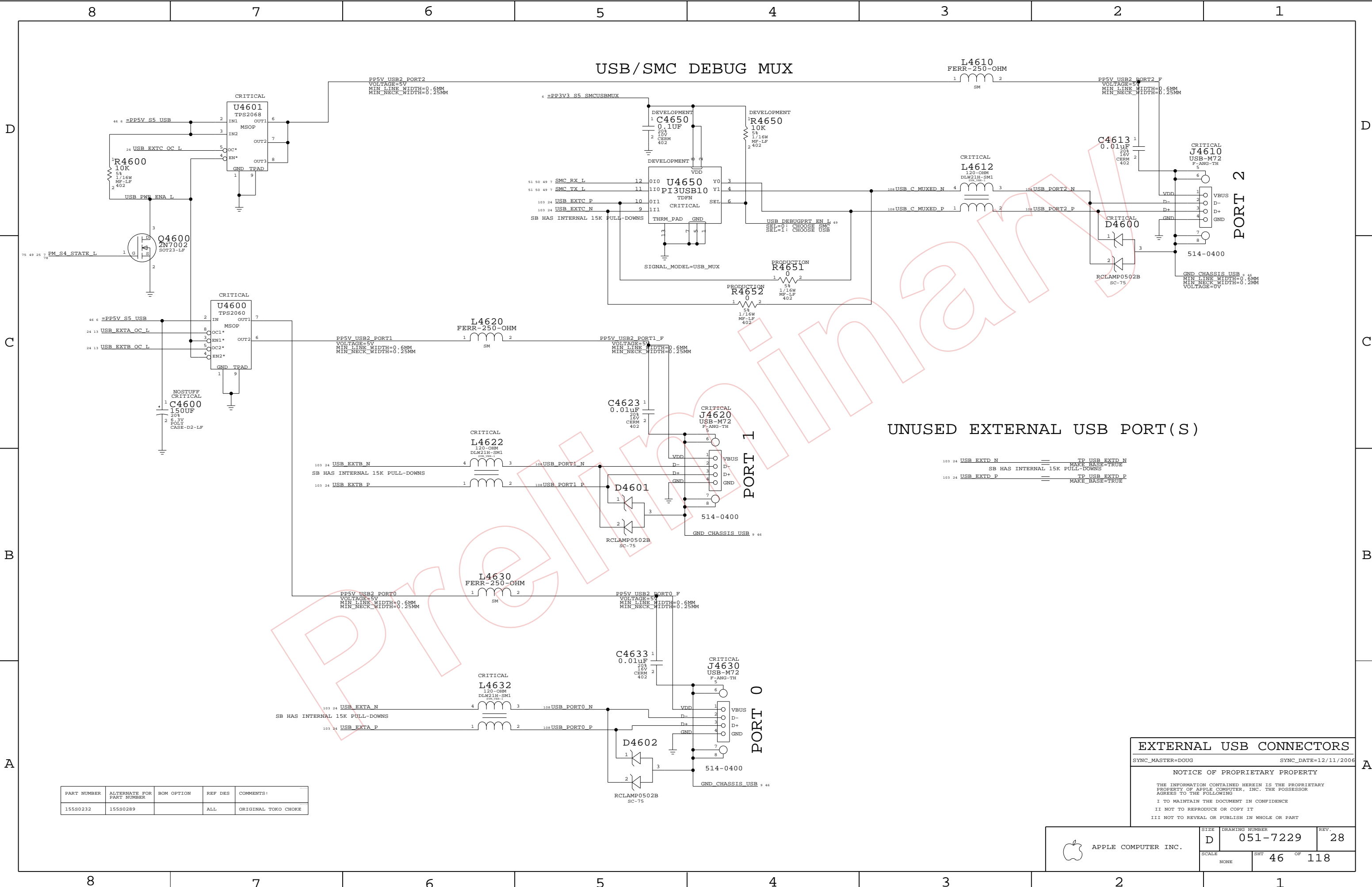
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SIZE D	DRAWING NUMBER 051-7229	REV. 28
SCALE NONE	SHT 42	OF 118





PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S0232	155S0289		ALL	ORIGINAL TOKO CHOKE

EXTERNAL USB CONNECTORS

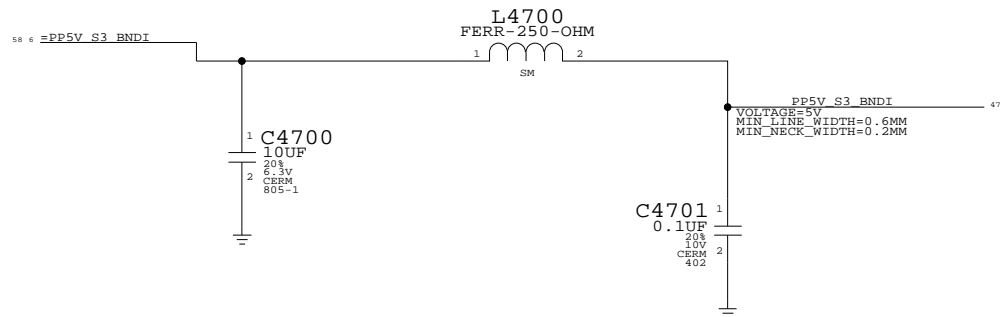
SYNC_MASTER=DOUG SYNC_DATE=12/11/2006

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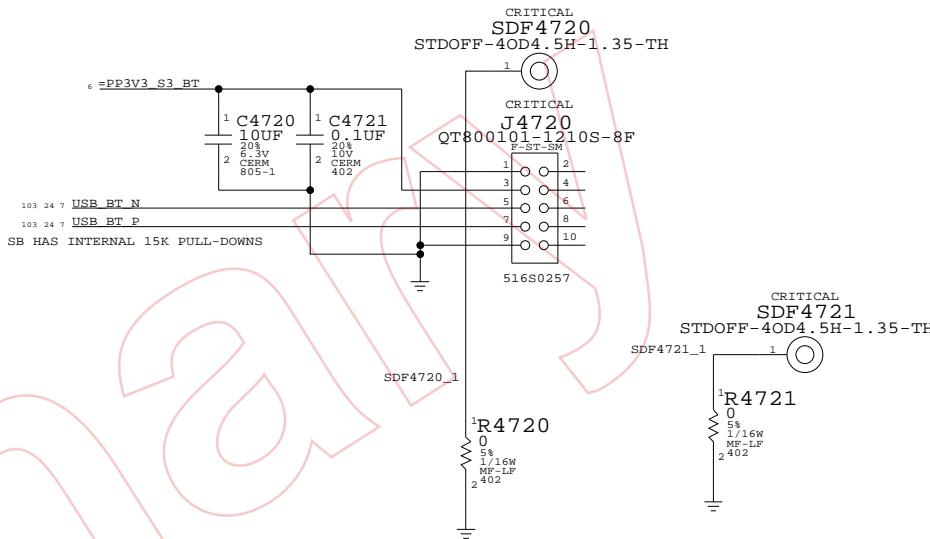
APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7229	REV. 28
	SCALE NONE	SHT 46	OF 118

CAMERA POWER FILTERING

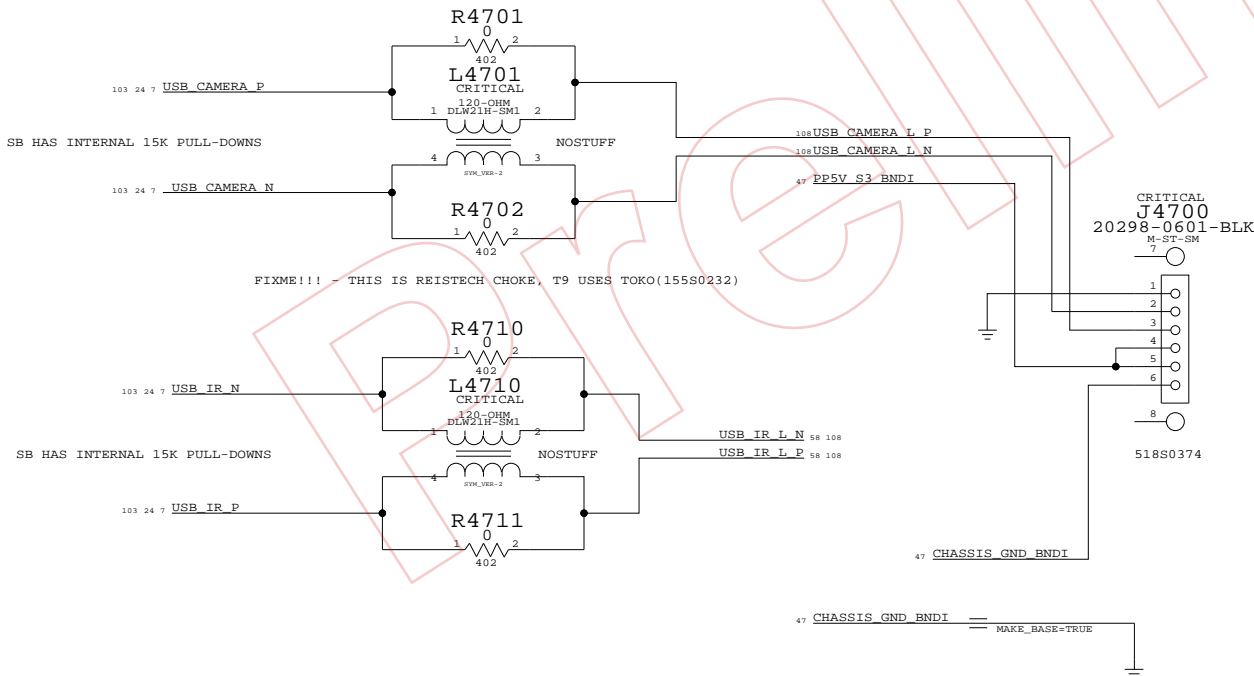


LAYOUT NOTE:
PLACE C4700, C4701 & L4700
NEAR J4700 PINS 4 AND 5 IN THE
ORDER LISTED, AND NOT ON
BOTH SIDES OF THE PIN.

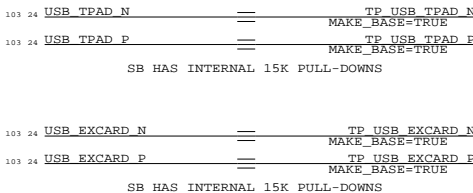
M13D (Bluetooth) Connector



CAMERA CONNECTOR

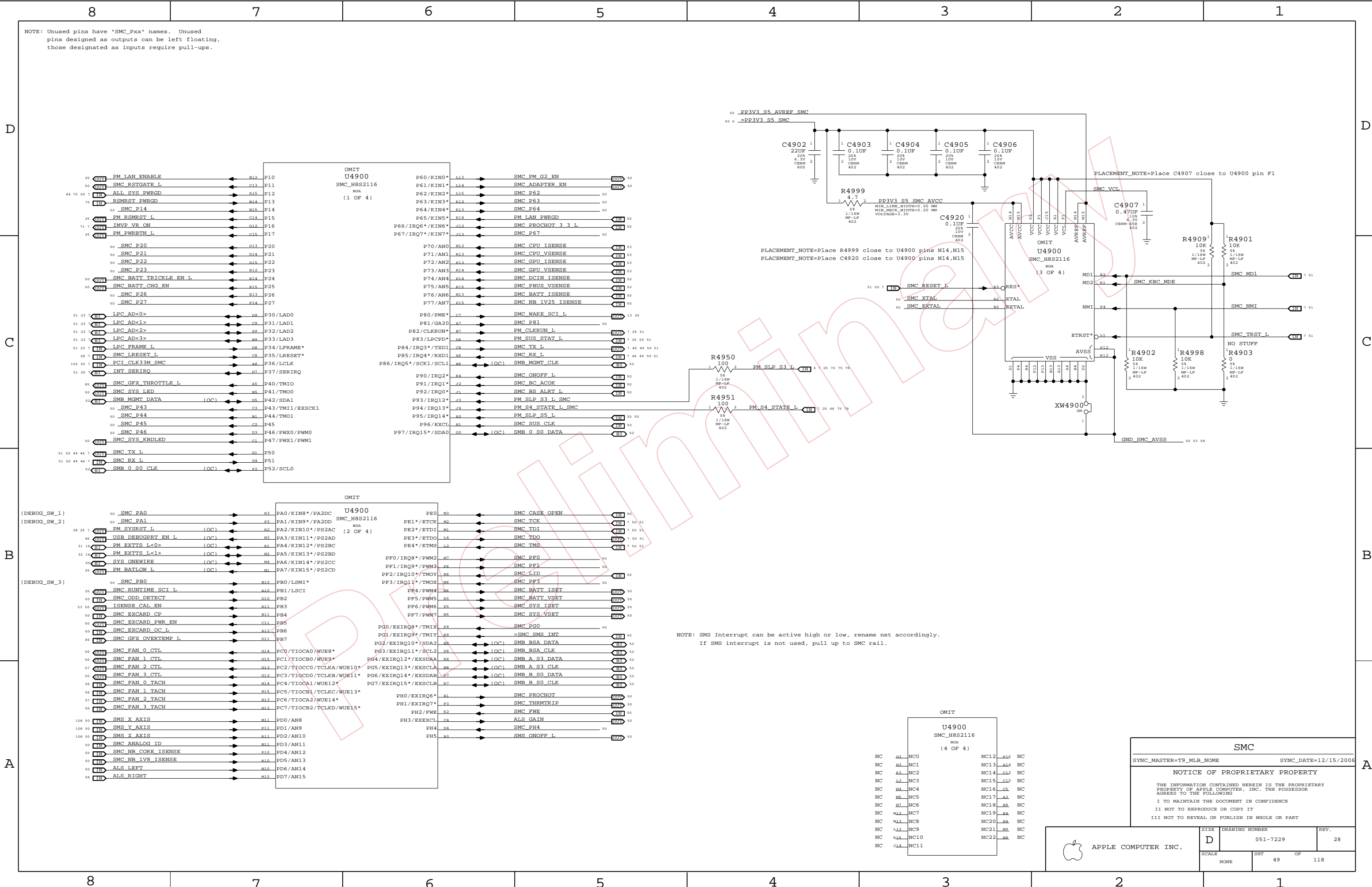


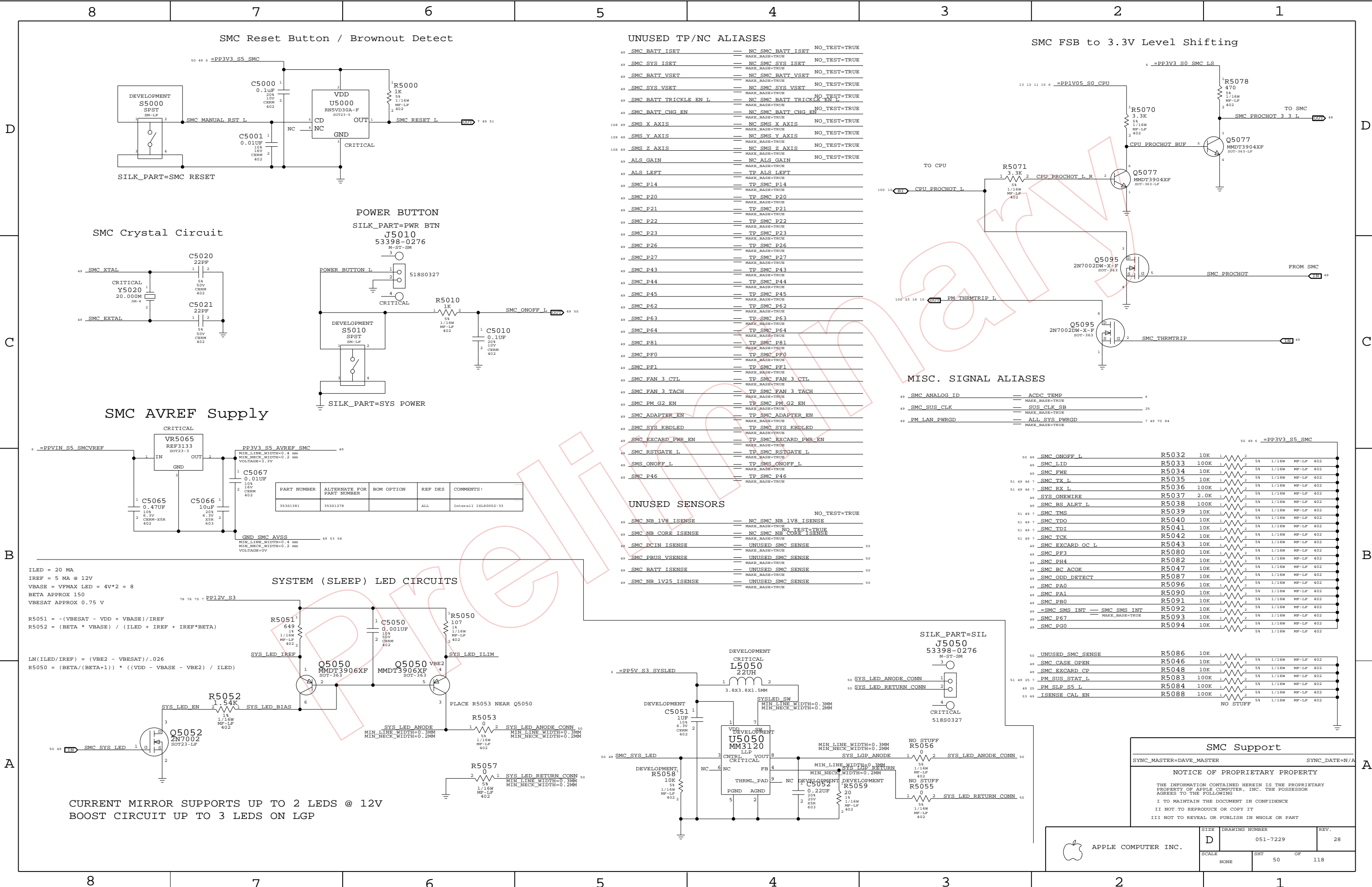
UNUSED INTERNAL USB PORTS

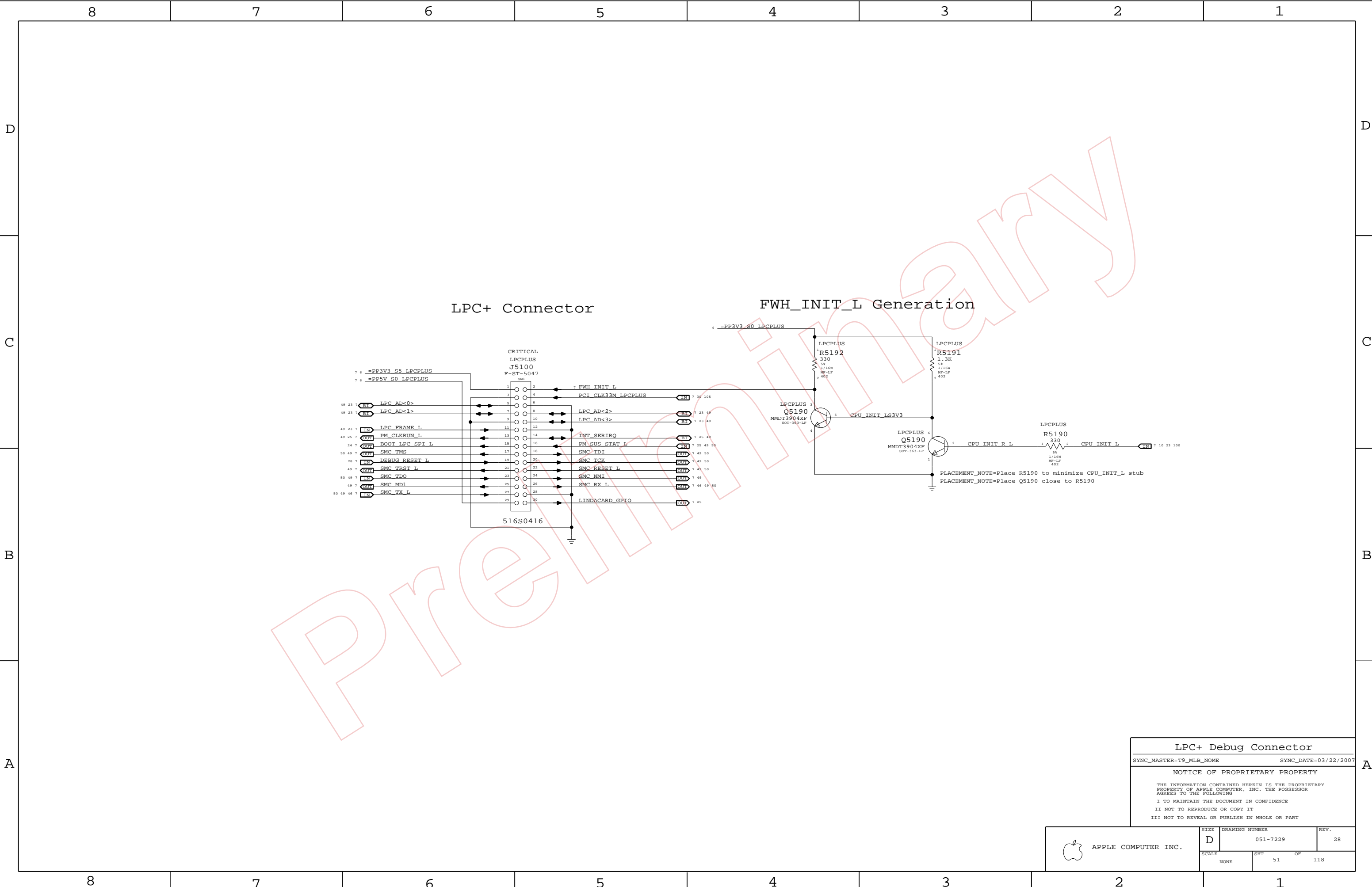


Internal USB Connections		
SYNC_MASTER=M78_MLB		SYNC_DATE=12/15/2006
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NONE		47	118







LPC+ Debug Connector

SYNC_MASTER=T9_MLB_NOME

SYNC_DATE=03/22/2007

NOTICE OF PROPRIETARY PROPERTY

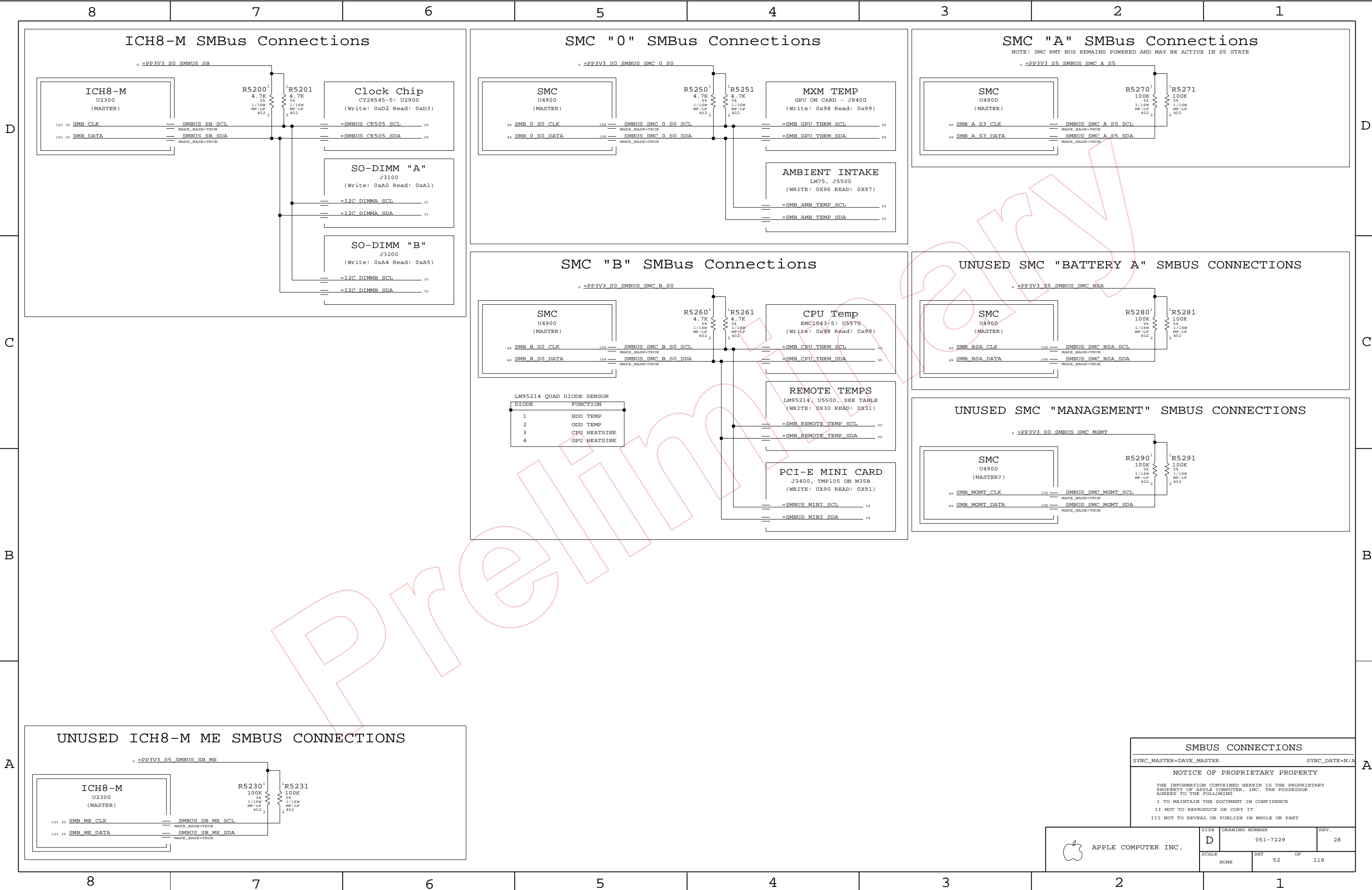
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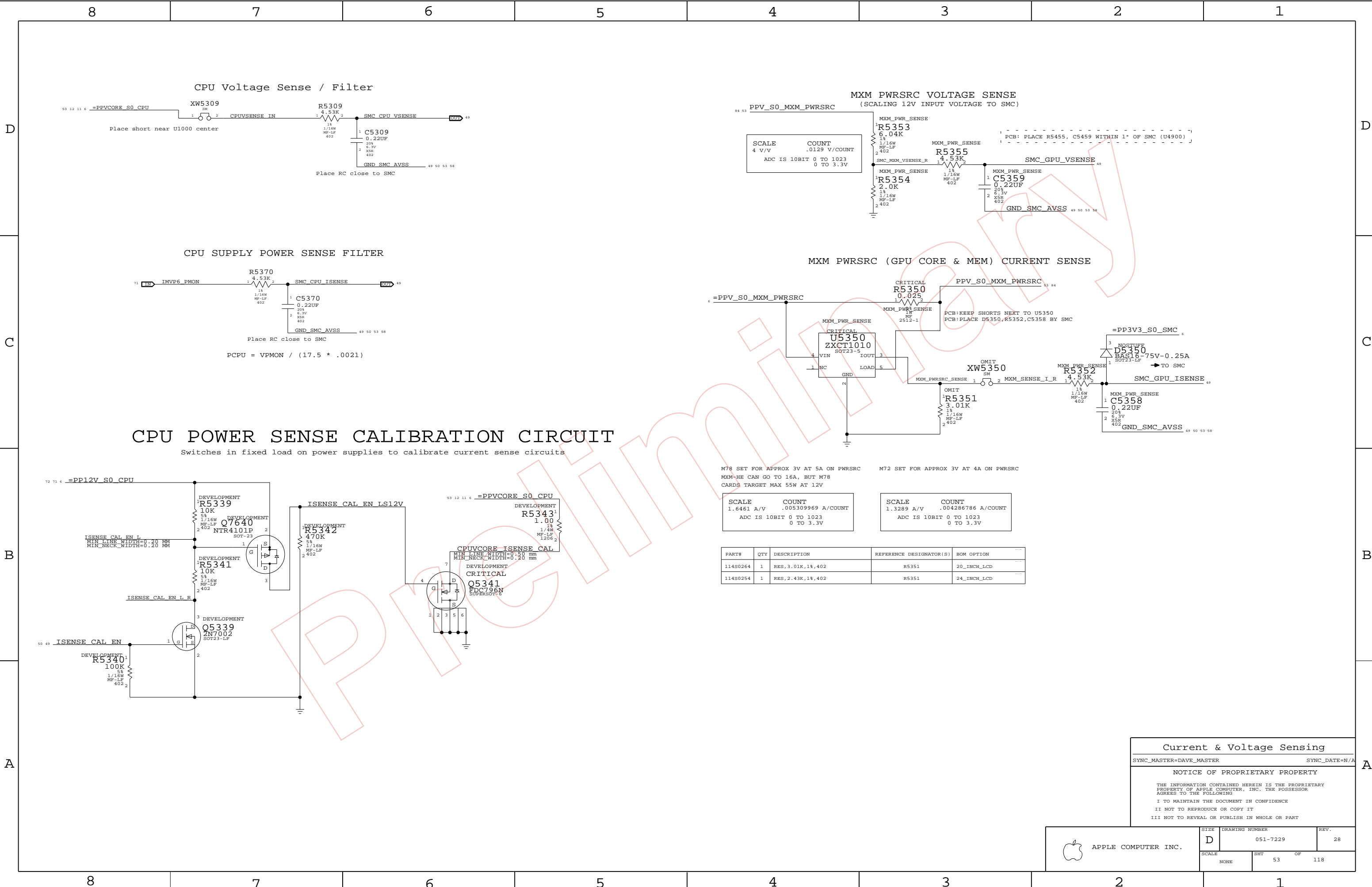
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SCALE		SHT	OF
NONE		51	118





CPU POWER SENSE CALIBRATION CIRCUIT

Switches in fixed load on power supplies to calibrate current sense circuits

M78 SET FOR APPROX 3V AT 5A ON PWRSRC
MXM-HE CAN GO TO 16A, BUT M78
CARDS TARGET MAX 55W AT 12V

SCALE	COUNT
1.6461 A/V	.005309969 A/COUNT
ADC IS 10BIT 0 TO 1023	0 TO 3.3V

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BCM OPTION
114S0264	1	RES,3.01K,1%,402	R5351	20_INCH_LCD
114S0254	1	RES,2.43K,1%,402	R5351	24_INCH_LCD

Current & Voltage Sensing

SYNC_MASTER=DAVE_MASTER SYNC_DATE=N/A

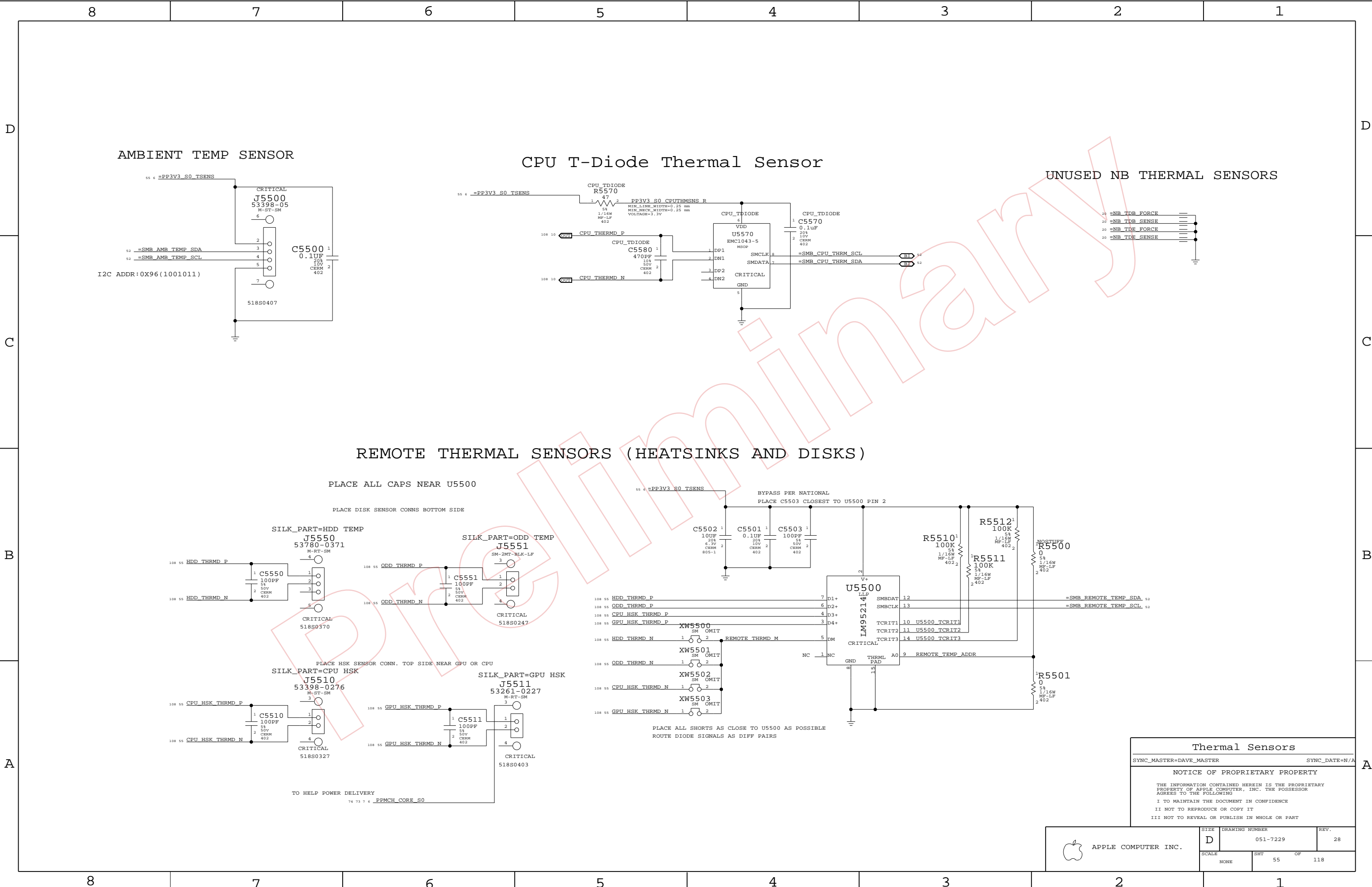
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D

C

B

A

D

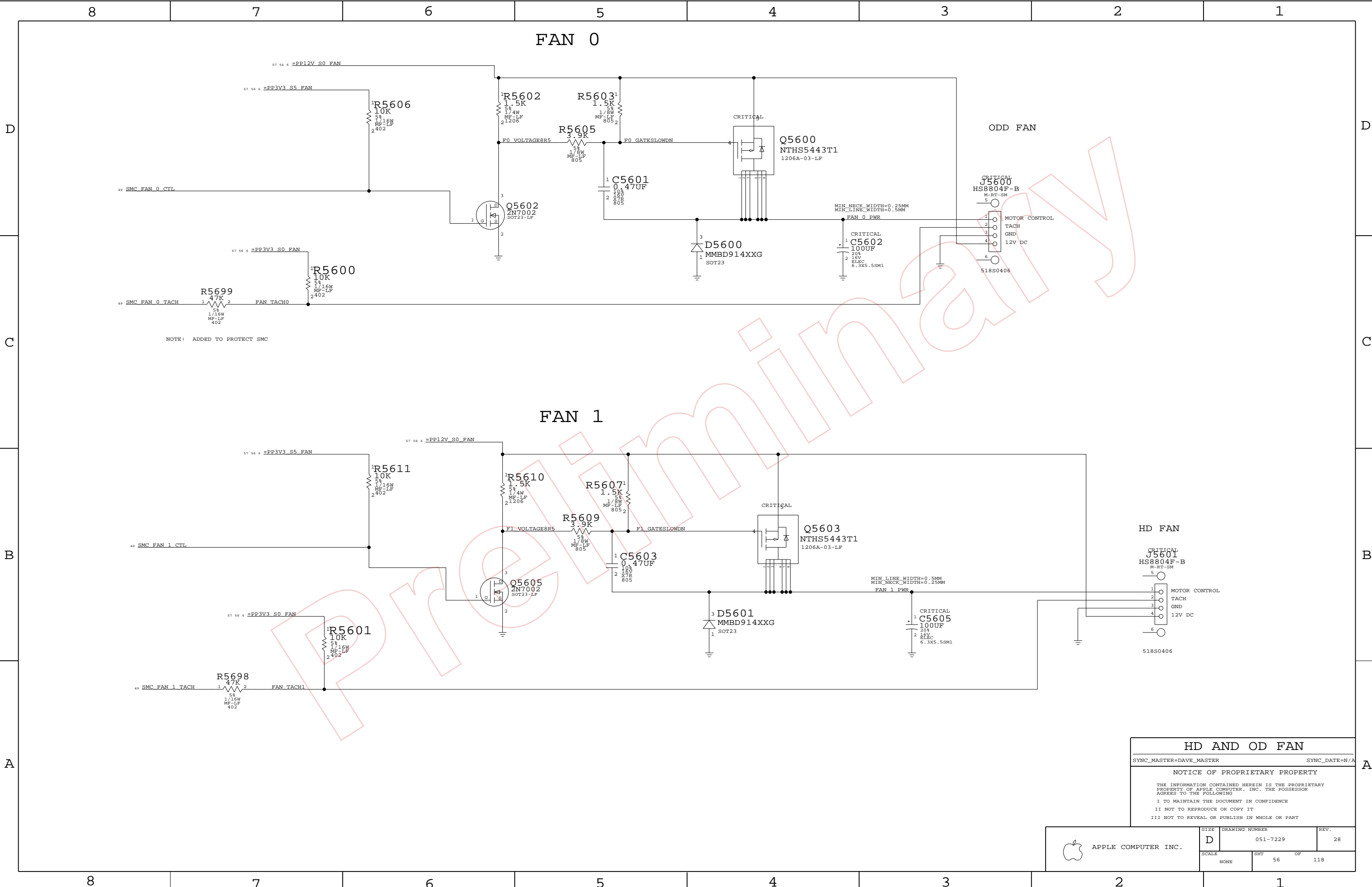
C

B

A

Thermal Sensors		
SYNC_MASTER=DAVE_MASTER		SYNC_DATE=N/A
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SCALE		SHT	OF
NONE		55	118



HD AND OD FAN

SYNC_MASTER=DAVE_MASTER SYNC_DATE=N/A

NOTICE OF PROPRIETARY PROPERTY

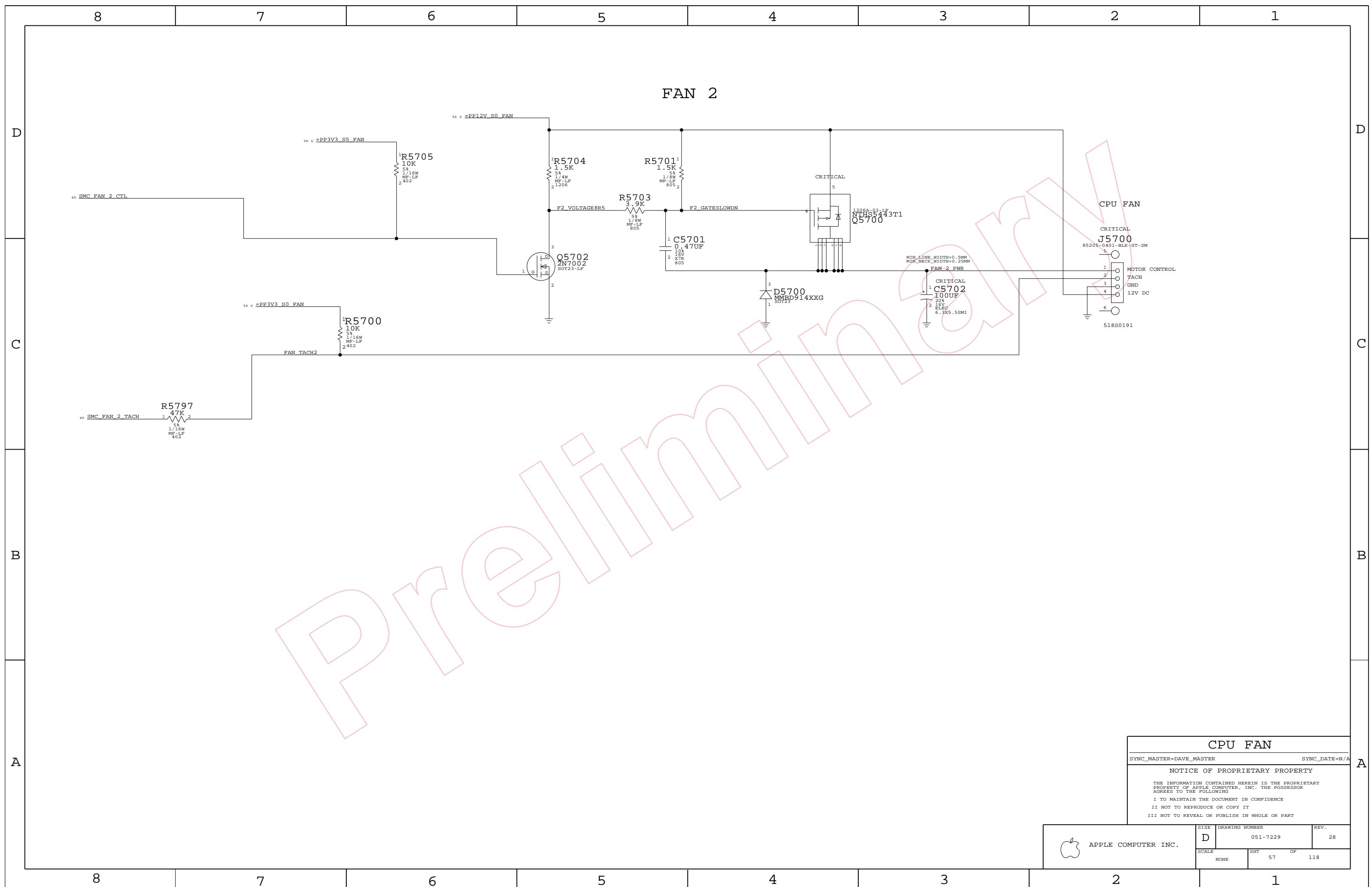
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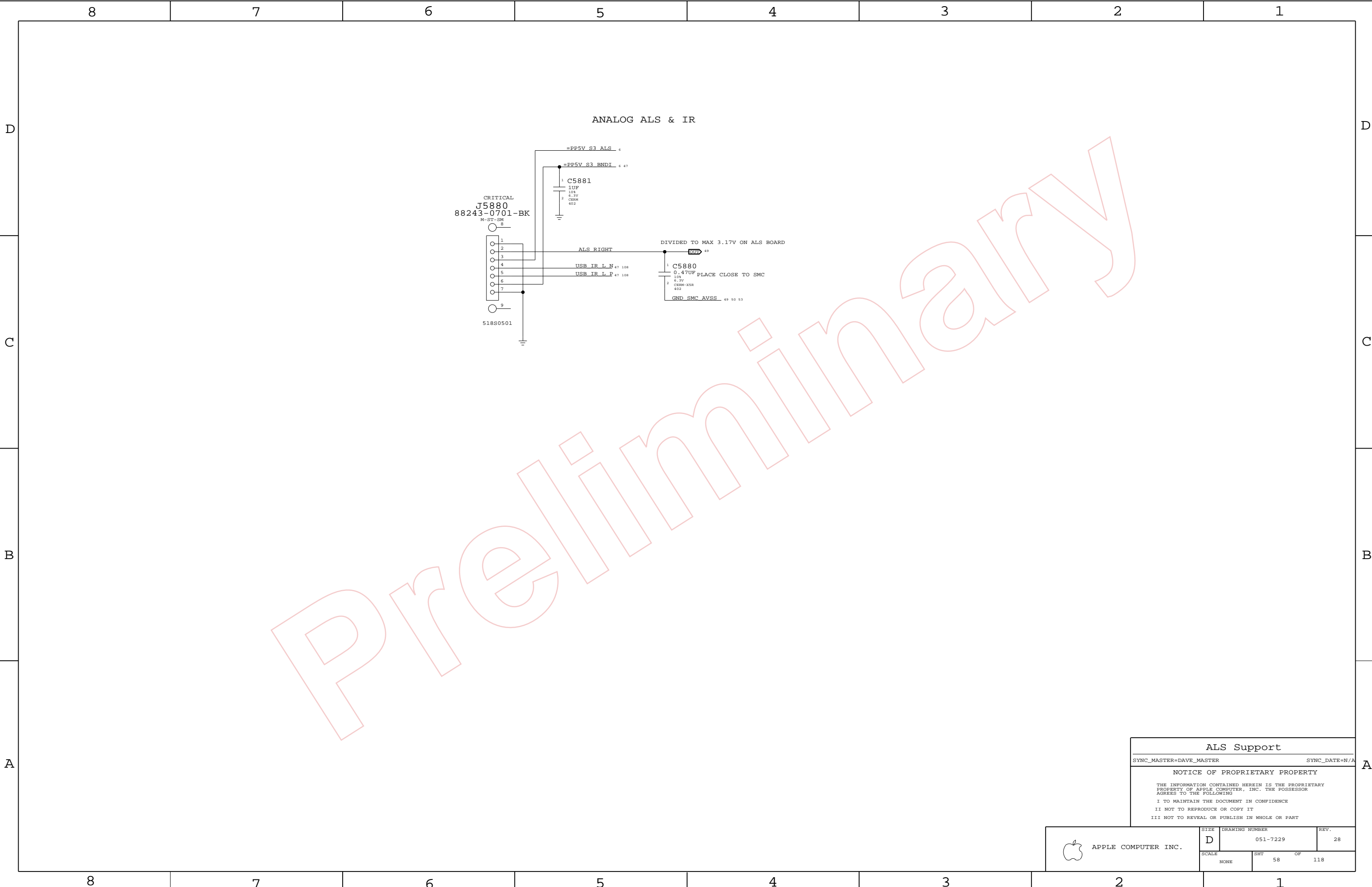
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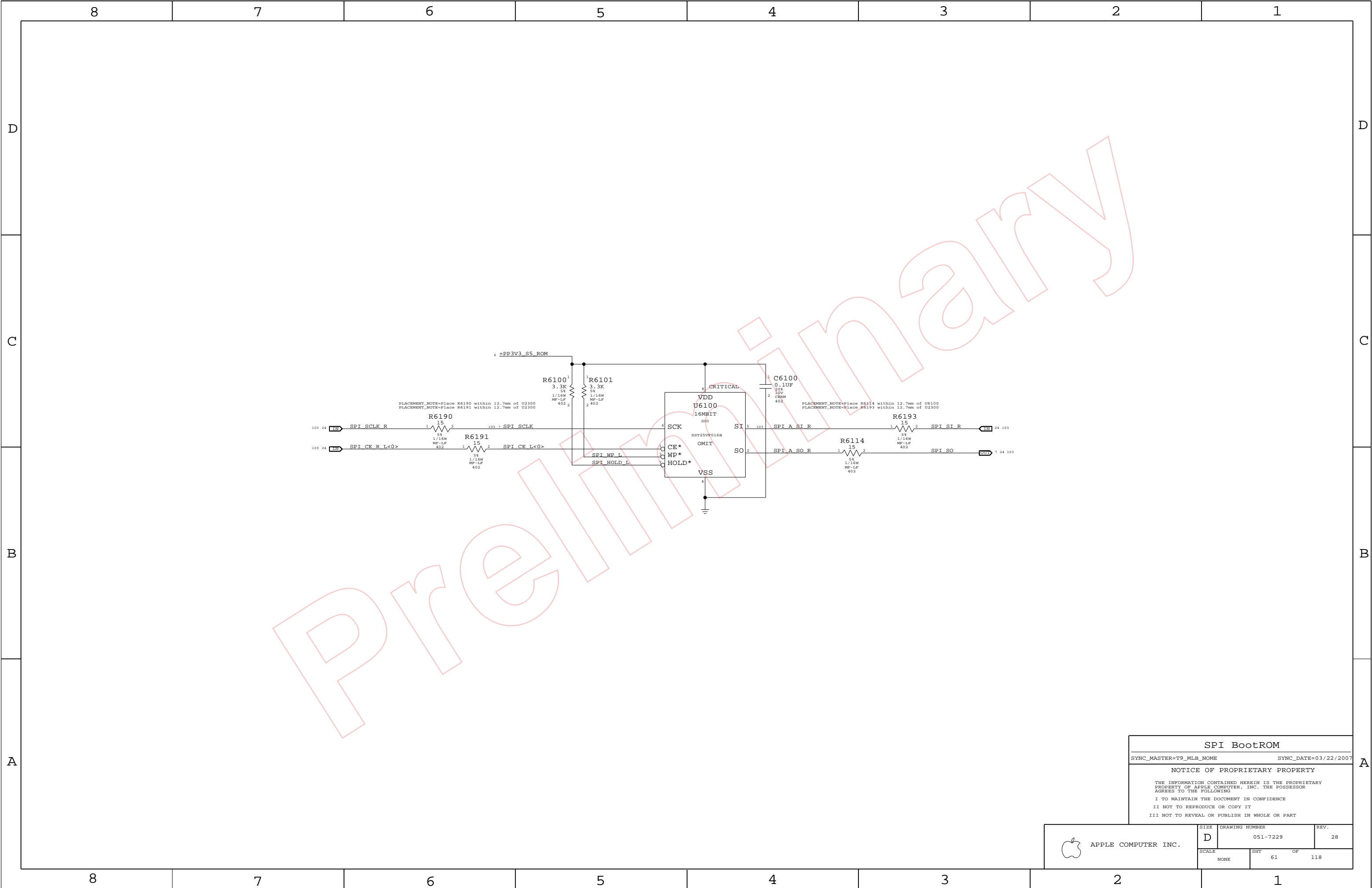
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

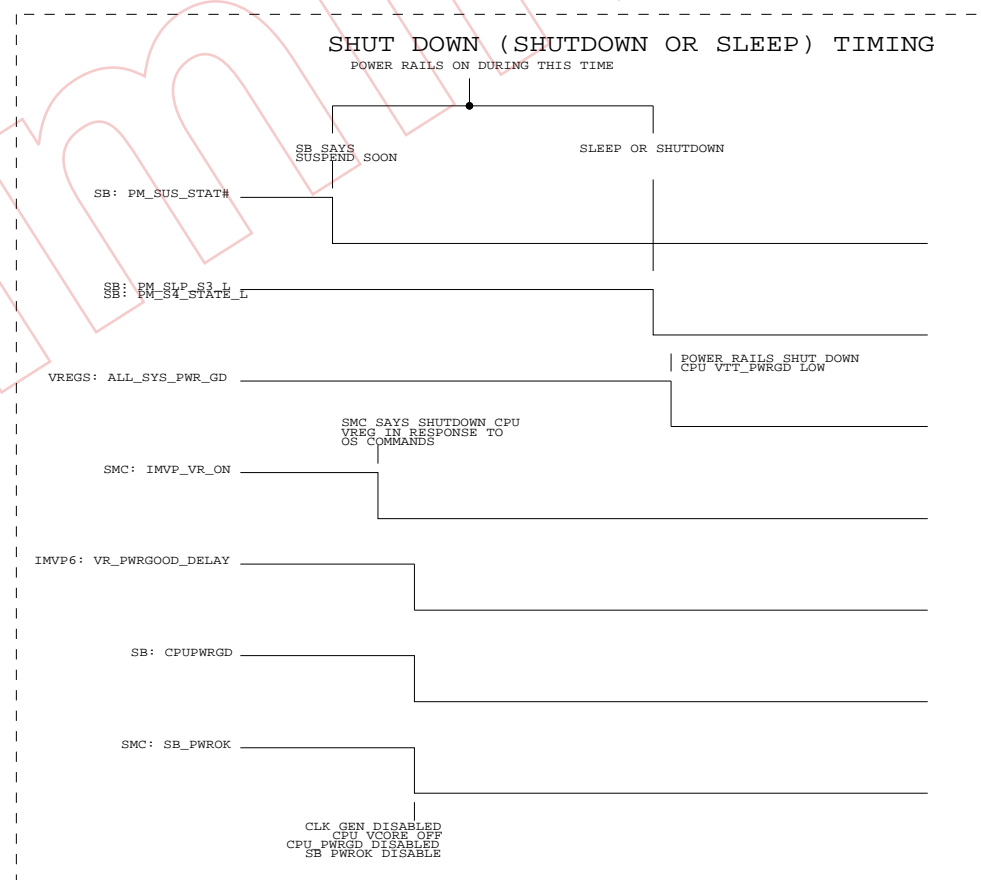
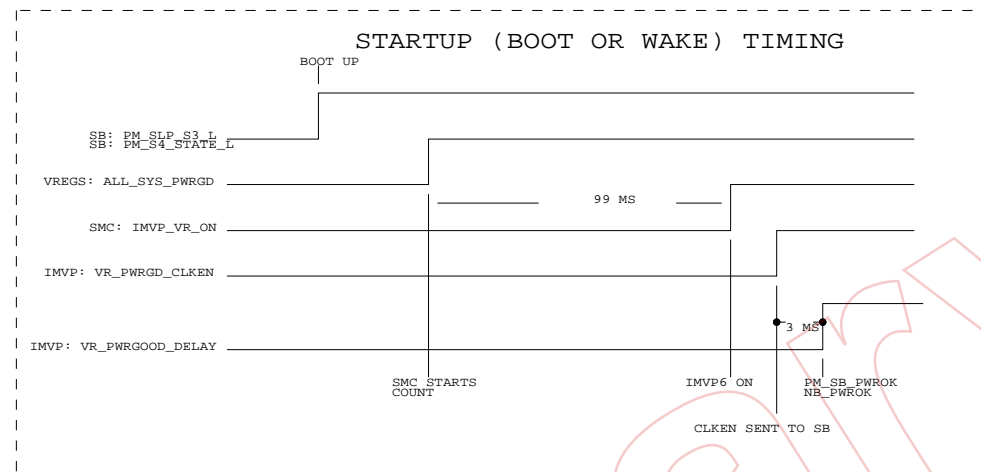
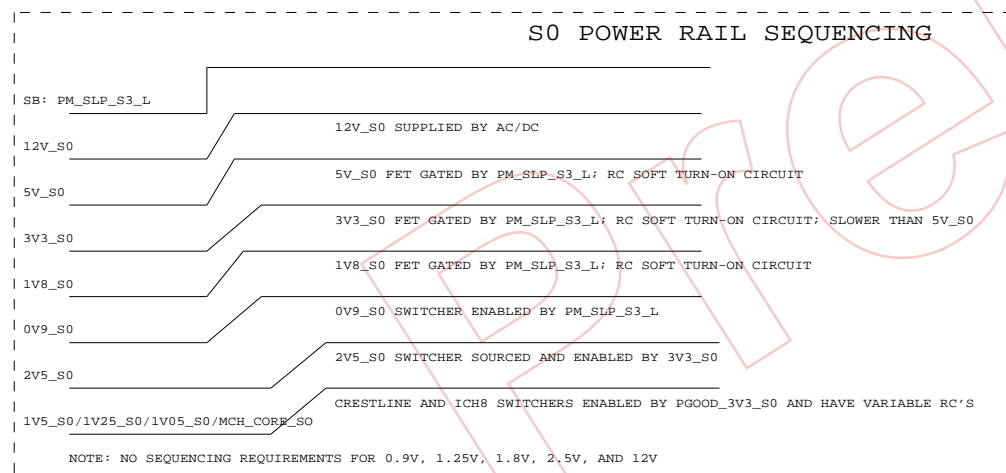
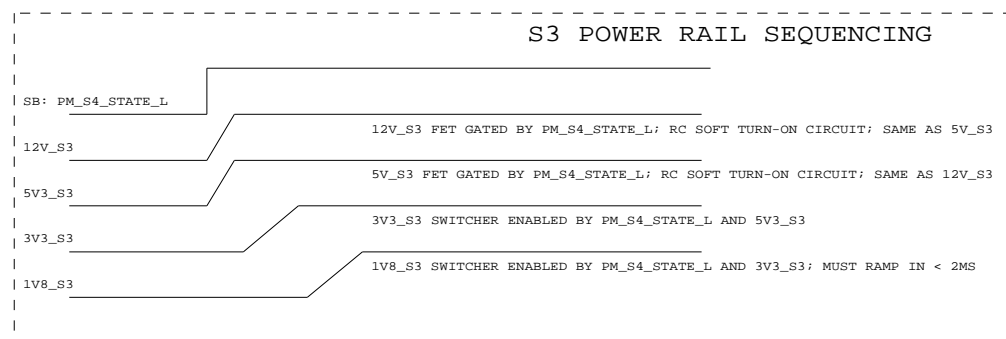
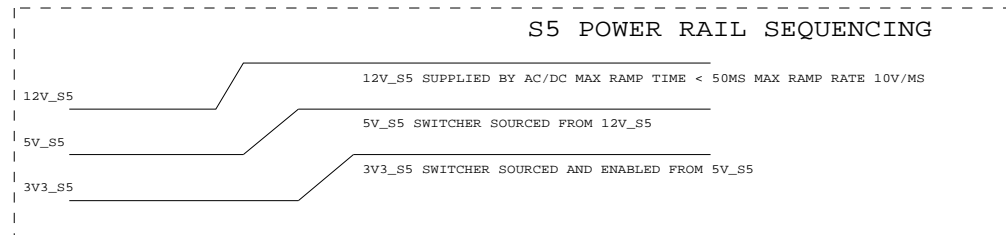
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NONE		56	118






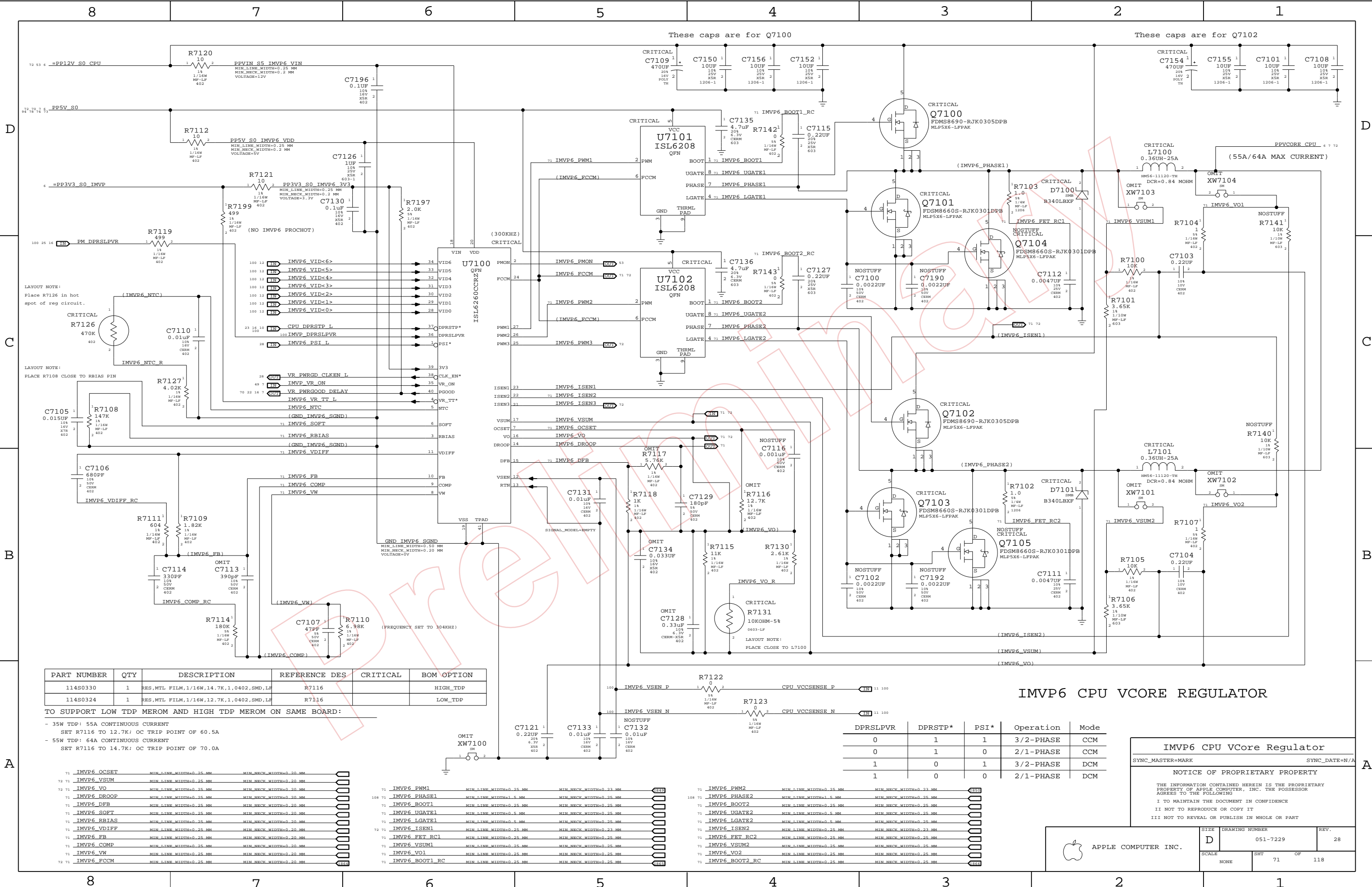
ALS Support		
SYNC_MASTER=DAVE_MASTER		SYNC_DATE=N/A
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SCALE NONE	SHT 58	OF 118





POWER SEQUENCING BLOCK DIAGRAM	
SYNC_MASTER=MARK	SYNC_DATE=N/A
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	D	051-7229	28
	SCALE	SHT OF	
	NONE	69	118



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0330	1	RES,MTL FILM,1/16W,14.7K,1,0402,SMD,LF	R7116		HIGH_TDP
114S0324	1	RES,MTL FILM,1/16W,12.7K,1,0402,SMD,LF	R7116		LOW_TDP

TO SUPPORT LOW TDP MEROM AND HIGH TDP MEROM ON SAME BOARD:

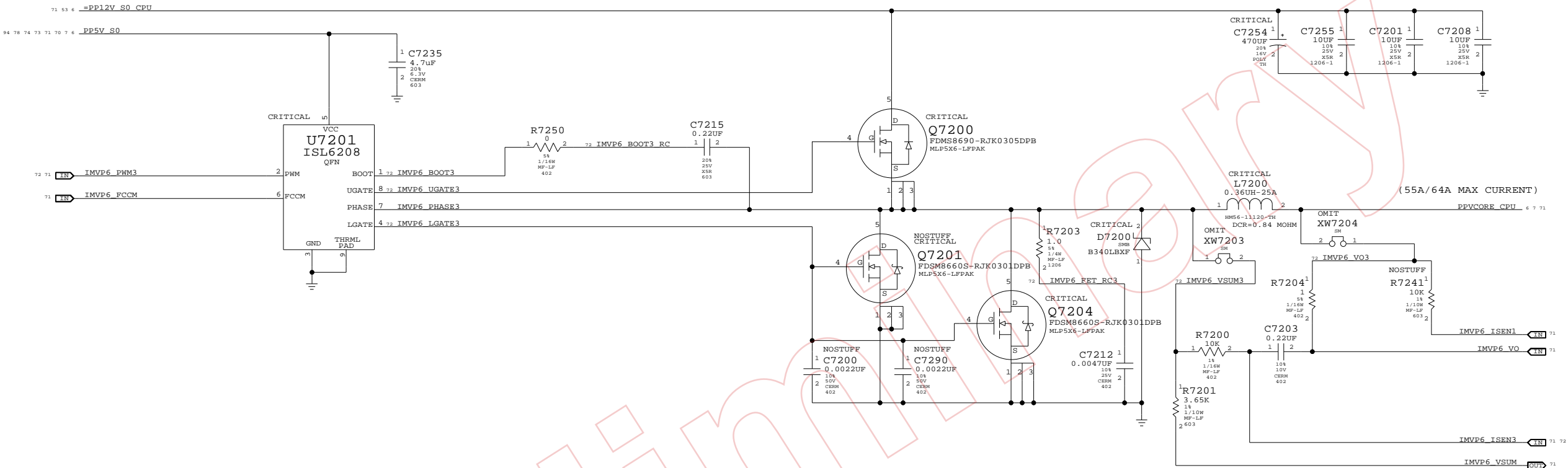
- 35W TDP: 55A CONTINUOUS CURRENT
SET R7116 TO 12.7K; OC TRIP POINT OF 60.5A
- 55W TDP: 64A CONTINUOUS CURRENT
SET R7116 TO 14.7K; OC TRIP POINT OF 70.0A

DPRSLPVR	DPRSTP*	PSI*	Operation	Mode
0	1	1	3/2-PHASE	CCM
0	1	0	2/1-PHASE	CCM
1	0	1	3/2-PHASE	DCM
1	0	0	2/1-PHASE	DCM

IMVP6 CPU VCore Regulator	
SYNC_MASTER=MARK	SYNC_DATE=N/A
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7229	28
SCALE		SHT	OF
NONE		71	118

IMVP6 CPU VCORE REGULATOR



72	71	IMVP6_PWM3	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.25 MM	154
108	72	IMVP6_PHASE3	MIN_LINE_WIDTH=1.5 MM	MIN_NECK_WIDTH=0.25 MM	155
72	72	IMVP6_BOOT3	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.25 MM	156
72	72	IMVP6_UGATE3	MIN_LINE_WIDTH=0.5 MM	MIN_NECK_WIDTH=0.25 MM	157
72	72	IMVP6_LGATE3	MIN_LINE_WIDTH=0.5 MM	MIN_NECK_WIDTH=0.25 MM	158
72	71	IMVP6_ISEN3	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.25 MM	159
72	72	IMVP6_FET_RC3	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.25 MM	160
72	72	IMVP6_VSUM3	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.25 MM	161
72	72	IMVP6_VO3	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.25 MM	162
72	72	IMVP6_BOOT3_RC	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.25 MM	163

IMVP6 3RD PHASE

SYNC_MASTER=MARK

SYNC_DATE=N/A

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APPLE COMPUTER INC.

SIZE D

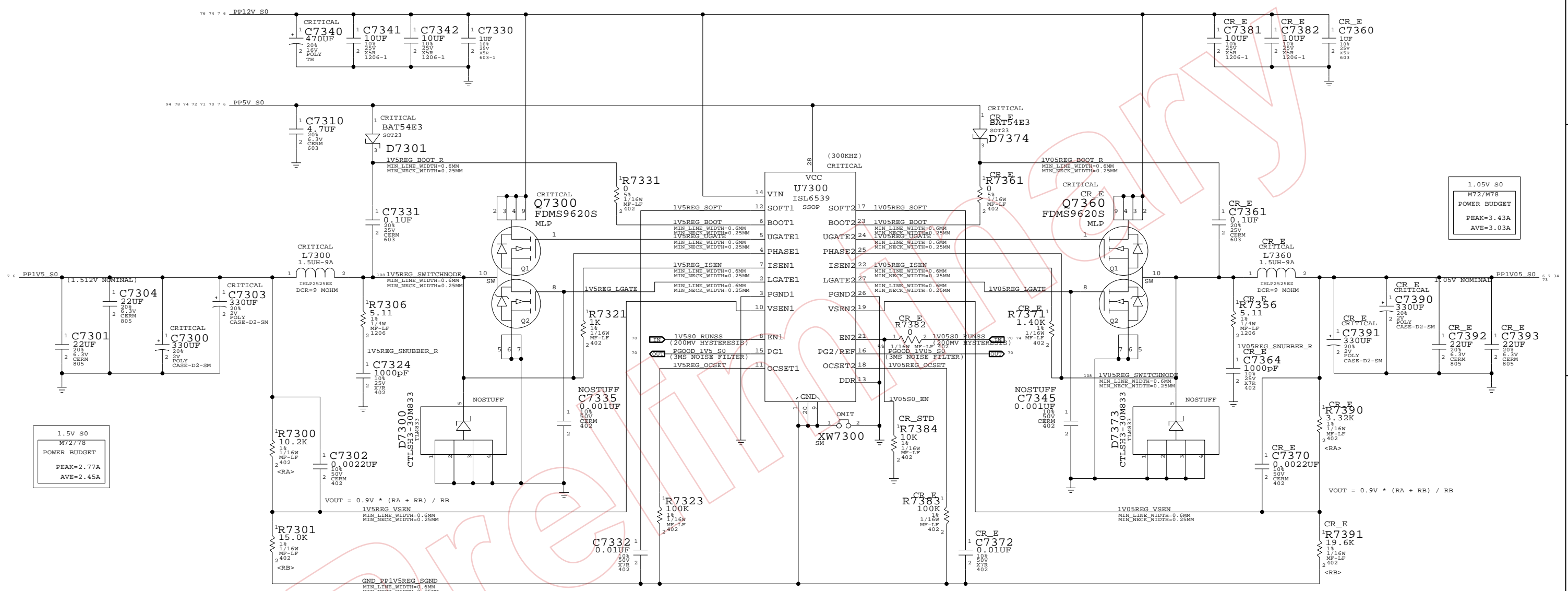
DRAWING NUMBER 051-7229

REV. 28

SCALE NONE

SHT 72 OF 118

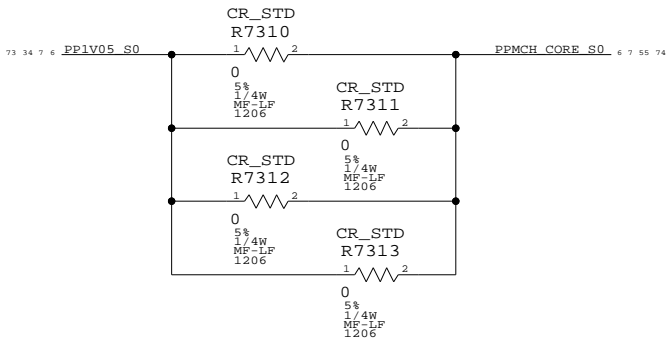
1.5V S0 & 1.05V S0 RAILS



1.5V S0
M72/78
POWER BUDGET
PEAK=2.77A
AVE=2.45A

1.05V S0
M72/M78
POWER BUDGET
PEAK=3.43A
AVE=3.03A

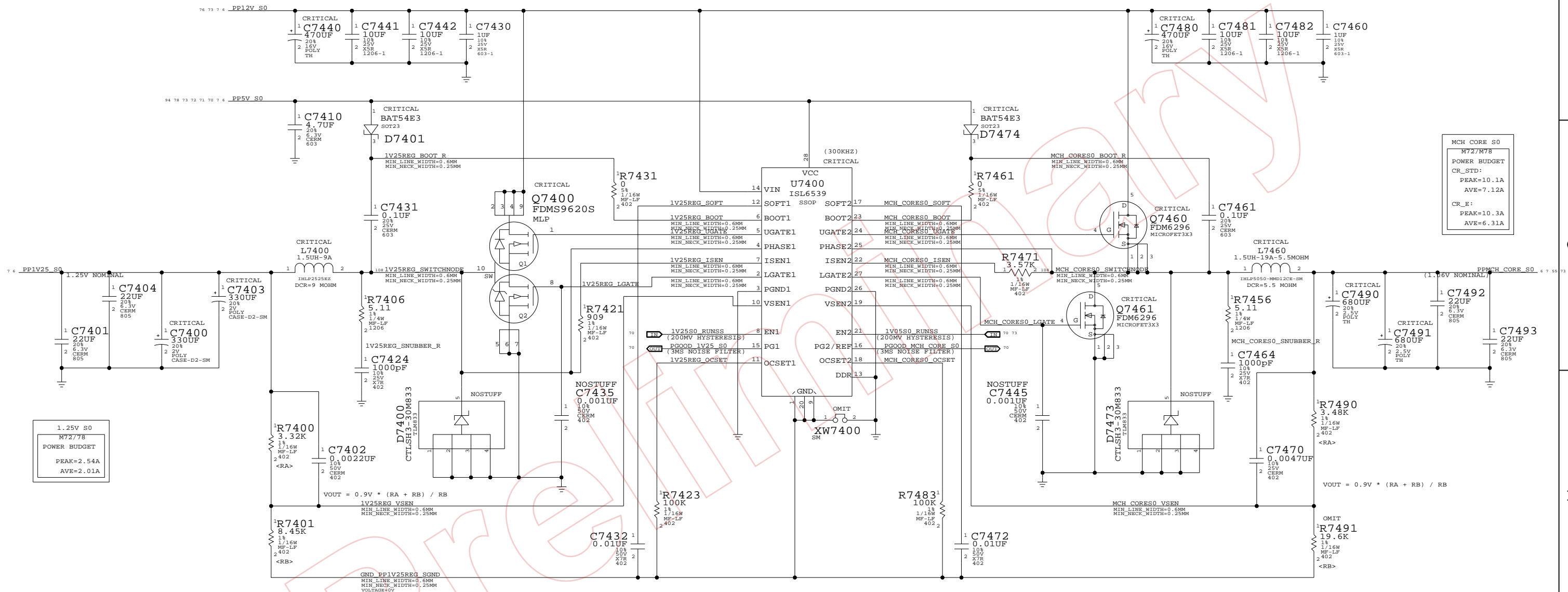
PLANE SHORTING RESISTORS



1.5V / 1.05V SUPPLIES
SYNC_MASTER=MARK SYNC_DATE=N/A
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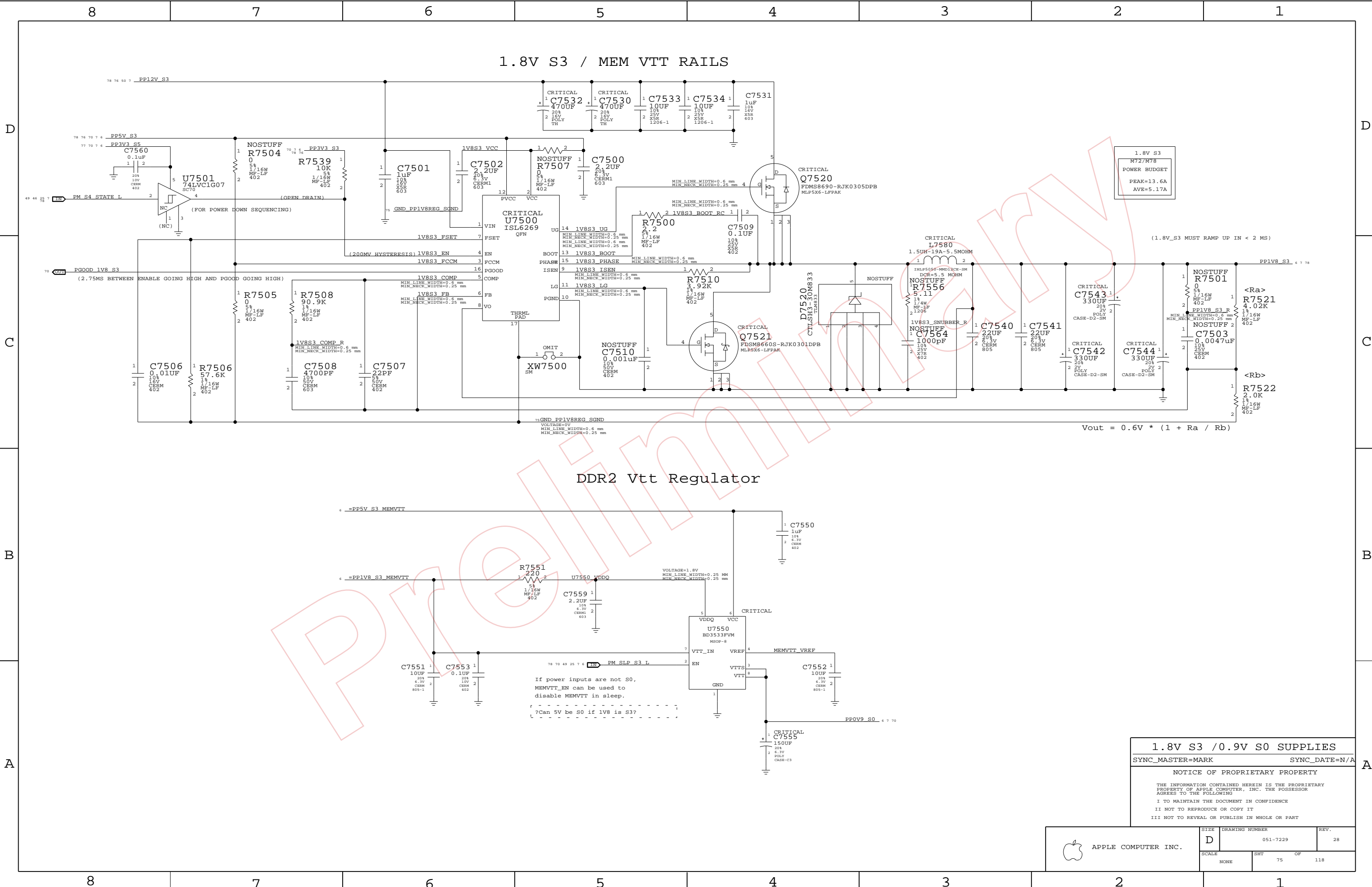
APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7229	REV. 28
	SCALE NONE	SHT 73 OF 118	

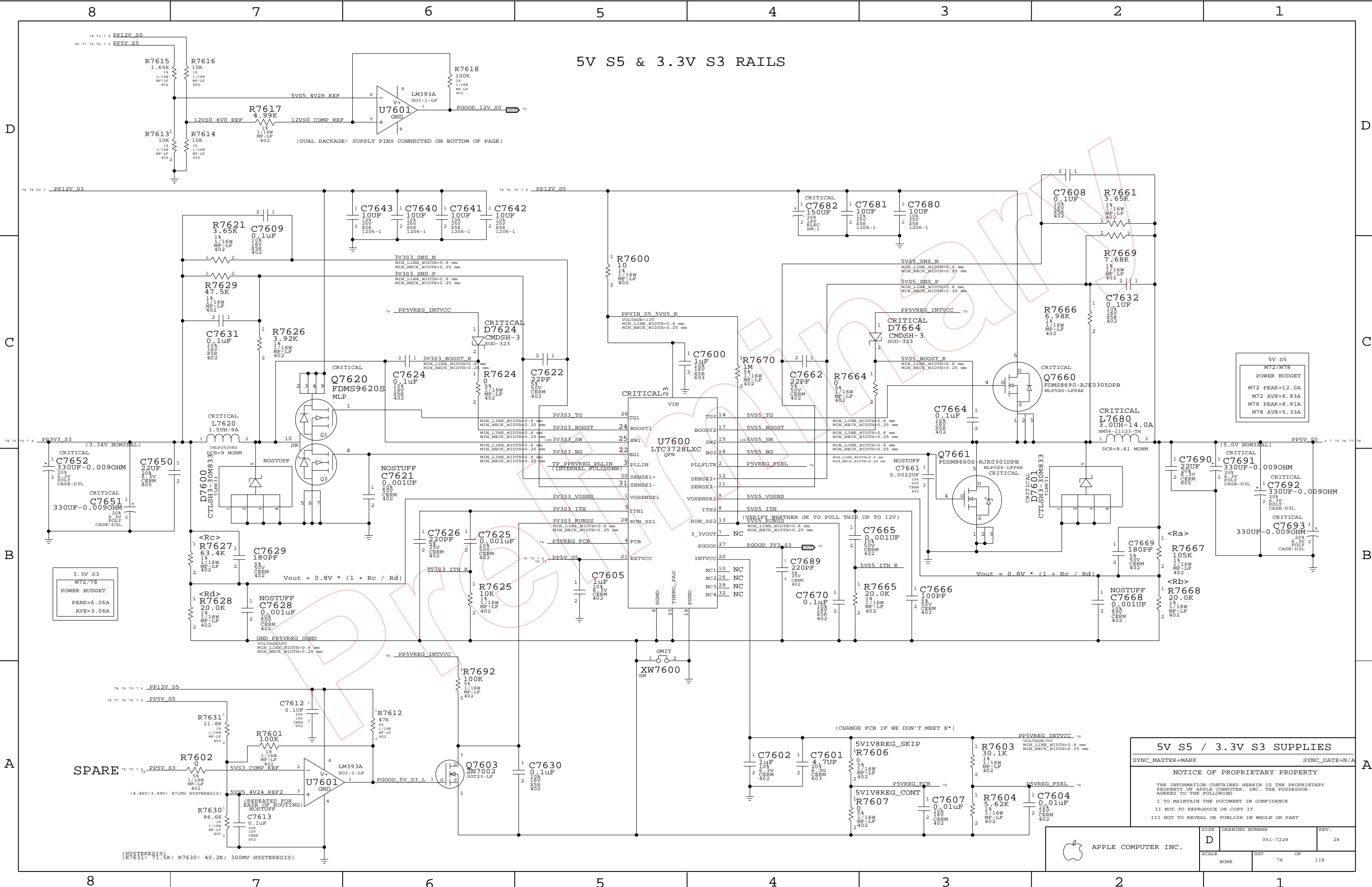
1.25V S0 & MCH CORE RAILS



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0342	1	RES,MTL FILM,1/16W,19.6K,1,0402,SMD,LF	R7491		CR_STD
114S0309	1	RES,MTL FILM,1/16W,8.66K,1,0402,SMD,LF	R7491		CR_E

1.25V / MCH CORE SUPPLIES	
SYNC_MASTER=MARK	SYNC_DATE=N/A
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5V S5 & 3.3V S3 RAILS

5V S5 / 3.3V S3 SUPPLIES

SYNC_MASTER=MARK SYNC_DATE=N/A

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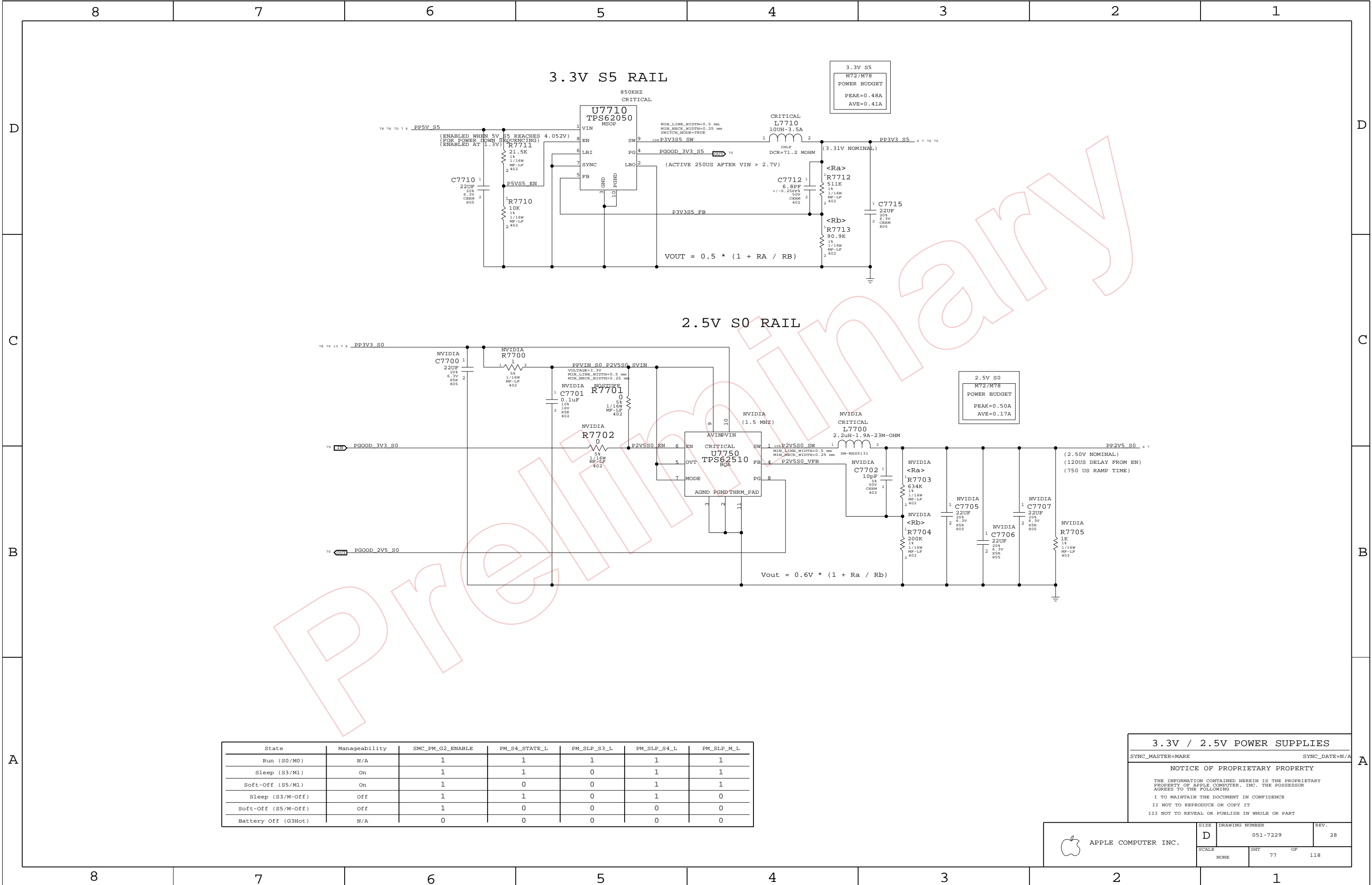
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SIZE	DRAWING NUMBER	REV.
D	051-7229	28
SCALE	SHT	OF
NONE	76	118

APPLE COMPUTER INC.



State	Manageability	SMC_PM_G2_ENABLE	PM_S4_STATE_L	PM_SLP_S3_L	PM_SLP_S4_L	PM_SLP_M_L
Run (S0/M0)	N/A	1	1	1	1	1
Sleep (S3/M1)	On	1	1	0	1	1
Soft-Off (S5/M1)	On	1	0	0	1	1
Sleep (S3/M-Off)	Off	1	1	0	1	0
Soft-Off (S5/M-Off)	Off	1	0	0	0	0
Battery Off (G3Hot)	N/A	0	0	0	0	0

3.3V / 2.5V POWER SUPPLIES

SYNC_MASTER=MARK

SYNC_DATE=N/A

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8

7

6

5

4

3

2

1

Page Notes

Power aliases required by this page:

- =PP12V_S0_MXM

- =PP5V_S0_MXM

- =PP1V8_S0_MXM

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)

MXM SPEC POWER REQUIREMENTS

(NOT NECESSARILY THE SAME FOR EVERY MODULE)

VOLTAGE	CURRENT	POWER
3V3	1.5 A	4.95 W
5V	0.5 A	2.5 W
2V5	0.5 A	1.25 W
1V8	3.5 A	6.3 W
PWR (12V)	UP TO 4 A	PLATFORM DEPENDENT

Note: PCI-E Lanes are reversed to untangle routes

Need to stuff config strap using BOM option NBCFG_PEG_REVERSE

Polarity is also inverted (Tx+ goes to Rx-) to untangle routes

APPLE P/N: 516S0562

J8400

AS0B52X-S43E-XF

F-RT-SM

(1 OF 2)

CRITICAL

PPV_S0_MXM_PWRSRC

53

VOLTAGE=12V

MIN_LINE_WIDTH=0.150MM

MIN_TRACE_WIDTH=0.250MM

C8401

22UF

20V

5.3V

805

C8400

22UF

20V

35V

ELEC

SM-LF

70

50

49

7

ALL_SYS_PWRGD

PRCNT2_L: RESERVED FOR FUTURE USE

KEY

PLACE CAPS NEAR NB

101	15	PEG R2D C P<0>	C8420	0.1uF	1	2	101	PEG R2D P<15>	40	PEX_TX15_L	37	PEG D2R N<0>	15	101
101	15	PEG R2D C N<0>	C8421	0.1uF	1	2	101	PEG R2D N<15>	42	PEX_TX15	39	PEG D2R P<0>	15	101
101	15	PEG R2D C P<1>	C8422	0.1uF	1	2	101	PEG R2D P<14>	44	PEX_TX14_L	43	PEG D2R N<1>	15	101
101	15	PEG R2D C N<1>	C8423	0.1uF	1	2	101	PEG R2D N<14>	46	PEX_TX14	45	PEG D2R P<1>	15	101
101	15	PEG R2D C P<2>	C8424	0.1uF	1	2	101	PEG R2D P<13>	48	PEX_TX13_L	47	PEG D2R N<2>	15	101
101	15	PEG R2D C N<2>	C8425	0.1uF	1	2	101	PEG R2D N<13>	50	PEX_TX13	49	PEG D2R P<2>	15	101
101	15	PEG R2D C P<3>	C8426	0.1uF	1	2	101	PEG R2D P<12>	52	PEX_TX12_L	51	PEG D2R N<3>	15	101
101	15	PEG R2D C N<3>	C8427	0.1uF	1	2	101	PEG R2D N<12>	54	PEX_TX12	52	PEG D2R P<3>	15	101
101	15	PEG R2D C P<4>	C8428	0.1uF	1	2	101	PEG R2D P<11>	56	PEX_TX11_L	53	PEG D2R N<4>	15	101
101	15	PEG R2D C N<4>	C8429	0.1uF	1	2	101	PEG R2D N<11>	58	PEX_TX11	54	PEG D2R P<4>	15	101
101	15	PEG R2D C P<5>	C8430	0.1uF	1	2	101	PEG R2D P<10>	60	PEX_TX10_L	55	PEG D2R N<5>	15	101
101	15	PEG R2D C N<5>	C8431	0.1uF	1	2	101	PEG R2D N<10>	62	PEX_TX10	56	PEG D2R P<5>	15	101
101	15	PEG R2D C P<6>	C8432	0.1uF	1	2	101	PEG R2D P<9>	64	PEX_TX9_L	57	PEG D2R N<6>	15	101
101	15	PEG R2D C N<6>	C8433	0.1uF	1	2	101	PEG R2D N<9>	66	PEX_TX9	58	PEG D2R P<6>	15	101
101	15	PEG R2D C P<7>	C8434	0.1uF	1	2	101	PEG R2D P<8>	68	PEX_TX8_L	59	PEG D2R N<7>	15	101
101	15	PEG R2D C N<7>	C8435	0.1uF	1	2	101	PEG R2D N<8>	70	PEX_TX8	60	PEG D2R P<7>	15	101
101	15	PEG R2D C P<8>	C8436	0.1uF	1	2	101	PEG R2D P<7>	72	PEX_TX7_L	61	PEG D2R N<8>	15	101
101	15	PEG R2D C N<8>	C8437	0.1uF	1	2	101	PEG R2D N<7>	74	PEX_TX7	62	PEG D2R P<8>	15	101
101	15	PEG R2D C P<9>	C8438	0.1uF	1	2	101	PEG R2D P<6>	76	PEX_TX6_L	63	PEG D2R N<9>	15	101
101	15	PEG R2D C N<9>	C8439	0.1uF	1	2	101	PEG R2D N<6>	78	PEX_TX6	64	PEG D2R P<9>	15	101
101	15	PEG R2D C P<10>	C8440	0.1uF	1	2	101	PEG R2D P<5>	80	PEX_TX5_L	65	PEG D2R N<10>	15	101
101	15	PEG R2D C N<10>	C8441	0.1uF	1	2	101	PEG R2D N<5>	82	PEX_TX5	66	PEG D2R P<10>	15	101
101	15	PEG R2D C P<11>	C8442	0.1uF	1	2	101	PEG R2D P<4>	84	PEX_TX4_L	67	PEG D2R N<11>	15	101
101	15	PEG R2D C N<11>	C8443	0.1uF	1</									

```
- =PP12V_S0_MXM
- =PP5V_S0_MXM
- =PP1V8_S0_MXM
```

BOM options provided by this page:
(NONE)

8

7

6

5

4

3

2

1

Page Notes

Power aliases required by this page:

- =PP12V_S0_MXM

- =PP5V_S0_MXM

- =PP1V8_S0_MXM

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)

MXM SPEC POWER REQUIREMENTS

(NOT NECESSARILY THE SAME FOR EVERY MODULE)

VOLTAGE	CURRENT	POWER
3V3	1.5 A	4.95 W
5V	0.5 A	2.5 W
2V5	0.5 A	1.25 W
1V8	3.5 A	6.3 W
PWR (12V)	UP TO 4 A	PLATFORM DEPENDENT

Note: PCI-E Lanes are reversed to untangle routes

Need to stuff config strap using BOM option NBCFG_PEG_REVERSE

Polarity is also inverted (Tx+ goes to Rx-) to untangle routes

APPLE P/N: 516S0562

J8400

AS0B52X-S43E-XF

F-RT-SM

(1 OF 2)

CRITICAL

PPV_S0_MXM_PWRSRC

53

VOLTAGE=12V

MIN_LINE_WIDTH=0.150MM

MIN_TRACE_WIDTH=0.250MM

C8401

22UF

20V

5.3V

805

C8400

22UF

20V

35V

ELEC

SM-LF

70

50

49

7

ALL_SYS_PWRGD

PRCNT2_L: RESERVED FOR FUTURE USE

KEY

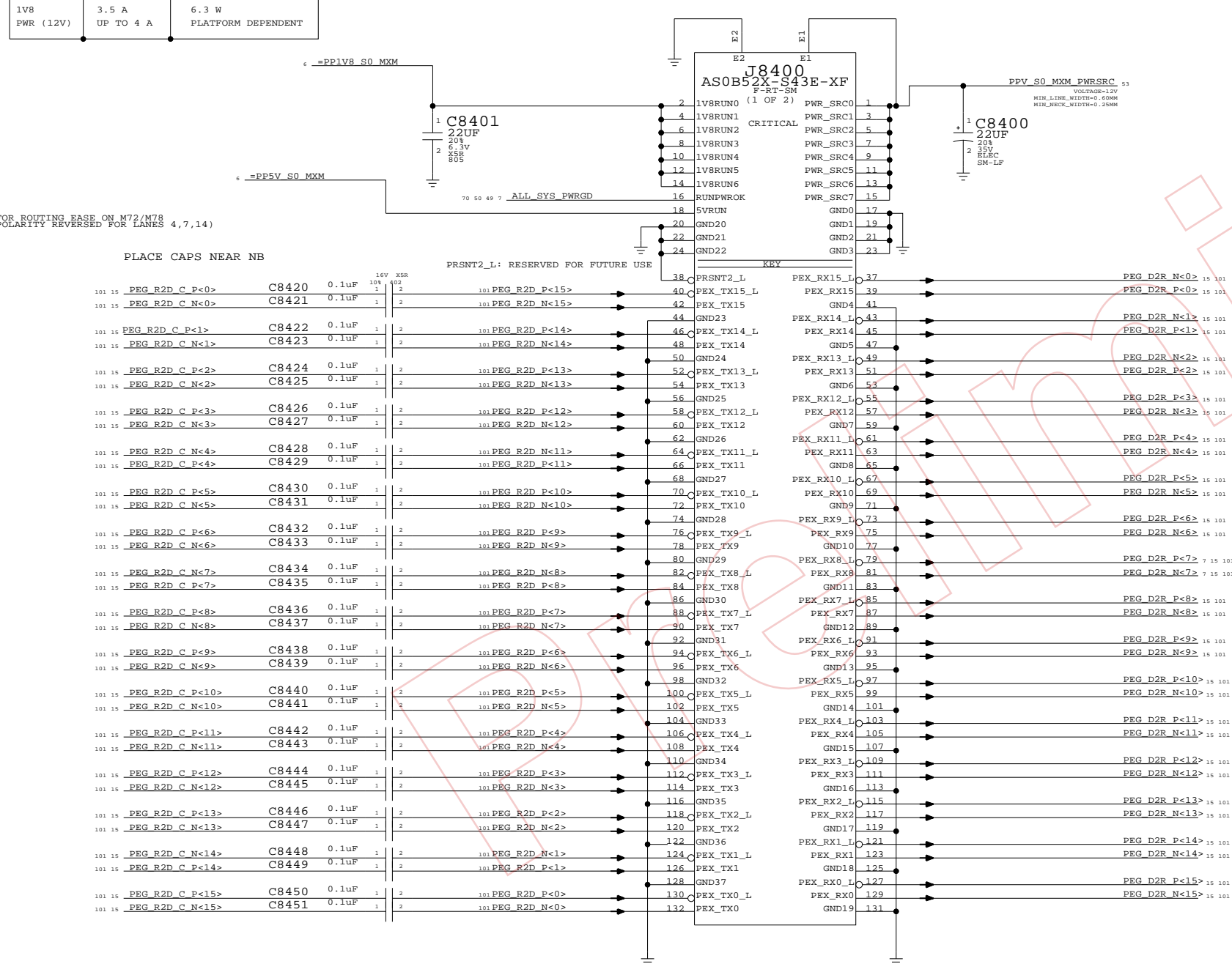
PLACE CAPS NEAR NB

101	15	PEG R2D C P<0>	C8420	0.1uF	1	2	101	PEG R2D P<15>	40	PEX_TX15_L	37	PEG D2R N<0>	15	101
101	15	PEG R2D C N<0>	C8421	0.1uF	1	2	101	PEG R2D N<15>	42	PEX_TX15	39	PEG D2R P<0>	15	101
101	15	PEG R2D C P<1>	C8422	0.1uF	1	2	101	PEG R2D P<14>	44	PEX_TX14_L	43	PEG D2R N<1>	15	101
101	15	PEG R2D C N<1>	C8423	0.1uF	1	2	101	PEG R2D N<14>	46	PEX_TX14	45	PEG D2R P<1>	15	101
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101	15	PEG R2D C P<4>	C8428	0.1uF	1	2	101	PEG R2D P<11>	56	PEX_TX11_L	53	PEG D2R N<4>	15	101
101	15	PEG R2D C N<4>	C8429	0.1uF	1	2	101	PEG R2D N<11>	58	PEX_TX11	54	PEG D2R P<4>	15	101
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101	15	PEG R2D C P<6>	C8432	0.1uF	1	2	101	PEG R2D P<9>	64	PEX_TX9_L	57	PEG D2R N<6>	15	101
101	15	PEG R2D C N<6>	C8433	0.1uF	1	2	101	PEG R2D N<9>	66	PEX_TX9	58	PEG D2R P<6>	15	101
101	15	PEG R2D C P<7>	C8434	0.1uF	1	2	101	PEG R2D P<8>	68	PEX_TX8_L	59	PEG D2R N<7>	15	101
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101	15	PEG R2D C N<10>	C8441	0.1uF	1	2	101	PEG R2D N<5>	82	PEX_TX5	66	PEG D2R P<10>	15	101
101	15	PEG R2D C P<11>	C8442	0.1uF	1	2	101	PEG R2D P<4>	84	PEX_TX4_L	67	PEG D2R N<11>	15	101
101	15	PEG R2D C N<11>	C8443	0.1uF	1</									

(NOT NECESSARILY THE SAME FOR EVERY MODULE)

VOLTAGE	CURRENT	POWER
3V3	1.5 A	4.95 W
5V	0.5 A	2.5 W
2V5	0.5 A	1.25 W
1V8	3.5 A	6.3 W
PWR (12V)	UP TO 4 A	PLATFORM DEPENDENT

APPLE P/N: 516S0562



(FOR ROUTING EASE ON M72/M78
(POLARITY REVERSED FOR LANES 0-2)

MXM PCI-E & PWR	
SYNC_MASTER=M78_MLB	SYNC_DATE=11/01/2006
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APPLE COMPUTER INC.

SIZE D	DRAWING NUMBER 051-7229	REV. 28
SCALE NONE	SHT 84 OF 118	

Power aliases required by this page:

- =PP3V3_S0_MXM
- =PP2V5_S0_MXM

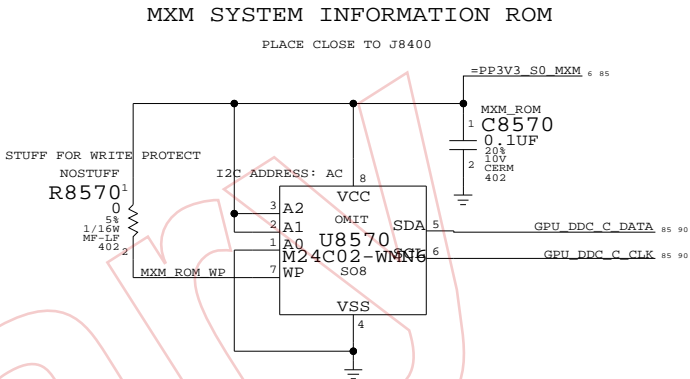
Signal aliases required by this page:

- =SMB_GPU_THRM_DATA
- =SMB_GPU_THRM_CLK

BOM options provided by this page:

24_INCH_LCD

MMX SPEC POWER REQUIREMENTS (NOT NECESSARILY THE SAME FOR EVERY MODULE)		
VOLTAGE	CURRENT	POWER
3V3	1.5 A	4.95 W
5V	0.5 A	2.5 W
2V5	0.5 A	1.25 W
1V8	3.5 A	6.3 W
PWR (12V)	UP TO 4 A	PLATFORM DEPENDENT



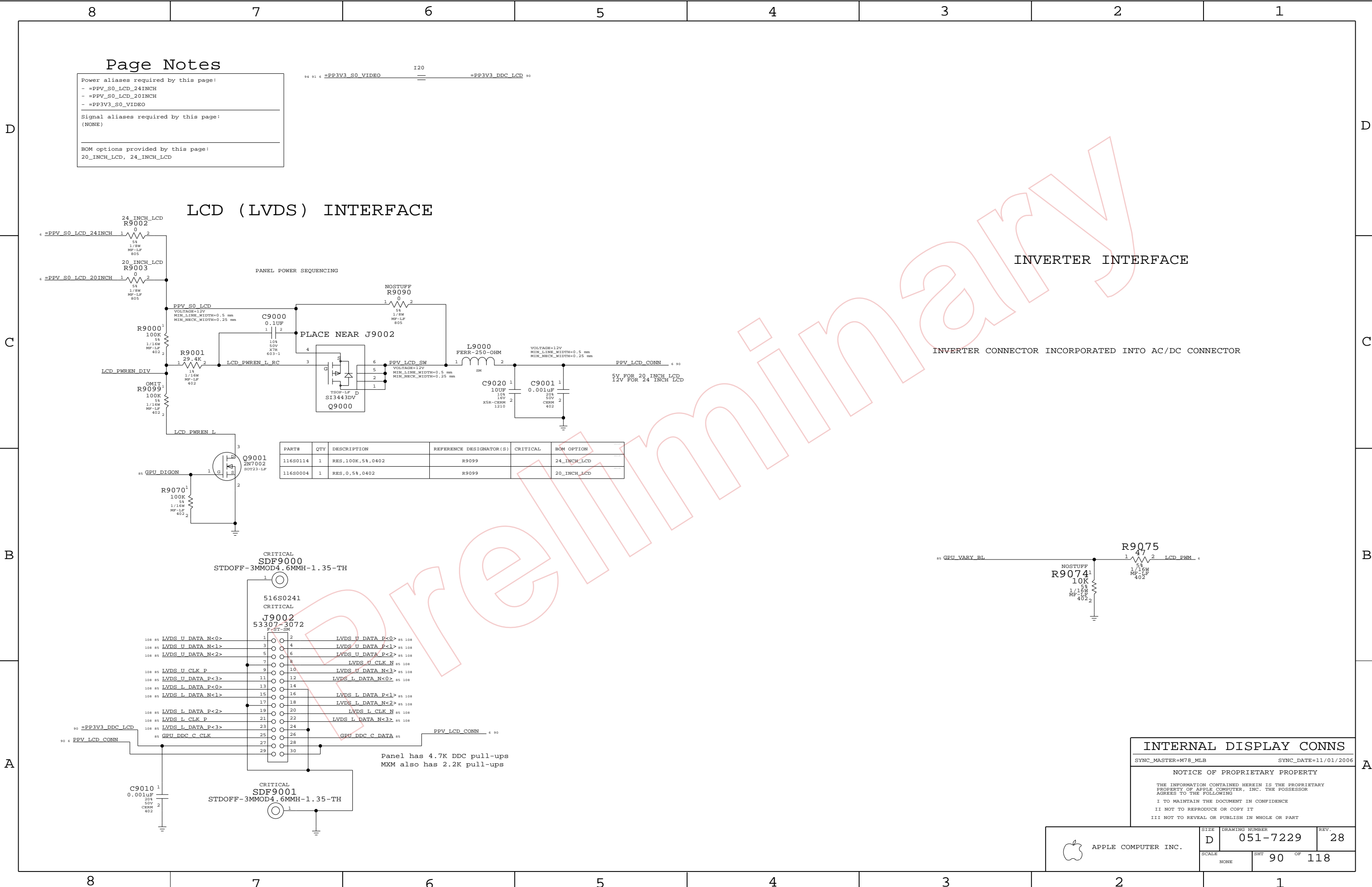
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MXM I/O
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SYNC_MASTER=M78_MLB                               SYNC_DATE=11/01/2006
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INTERNAL DISPLAY CONNS

SYNC_MASTER=M78_MLB SYNC_DATE=11/01/2006

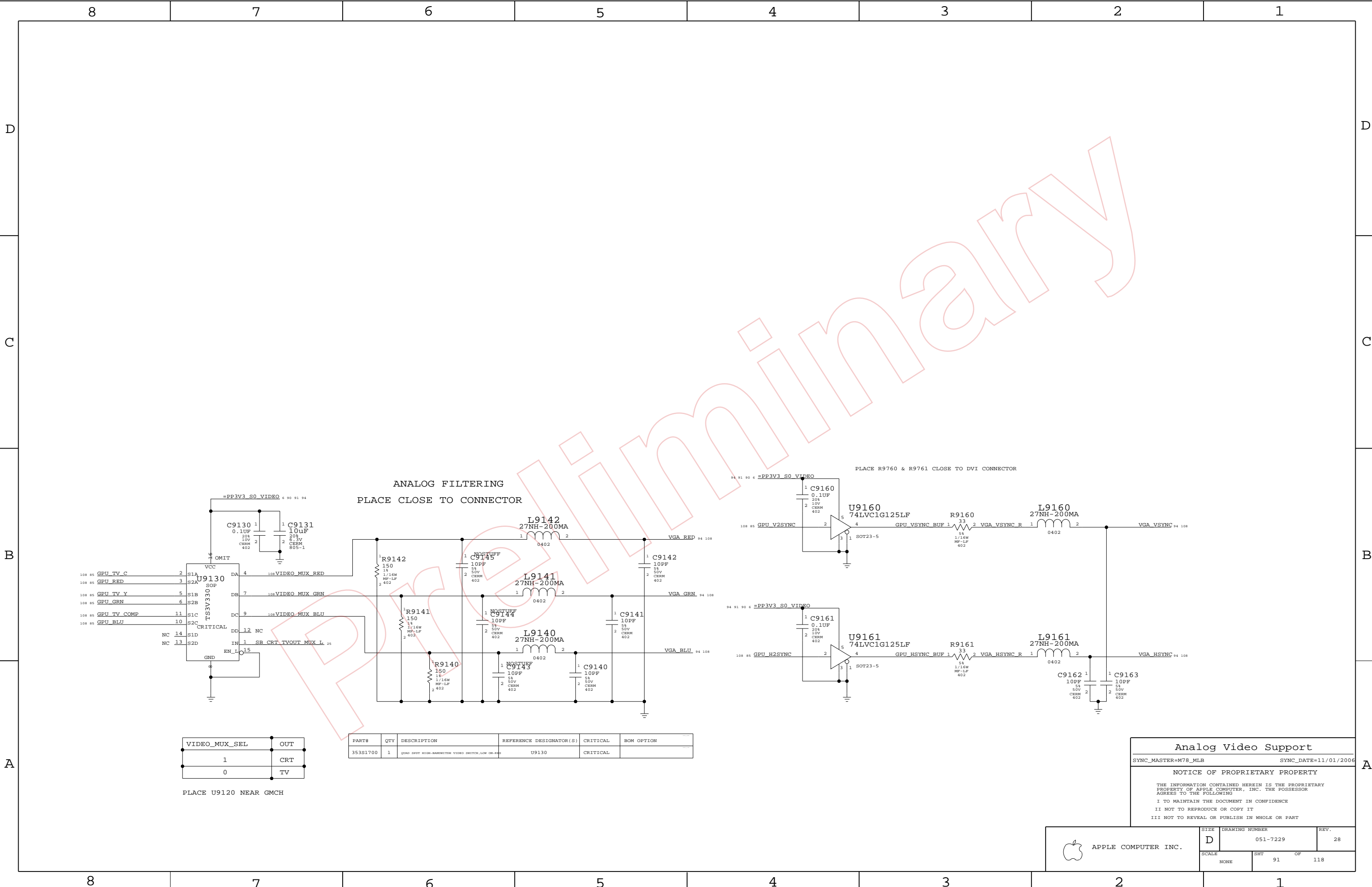
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VIDEO_MUX_SEL	OUT
1	CRT
0	TV

PLACE U9120 NEAR GMCH

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S1700	1	QUAD SPOT HIGH-BANDWIDTH VIDEO SWITCH, LOW ON-RES	U9130	CRITICAL	

Analog Video Support

SYNC_MASTER=M78_MLB SYNC_DATE=11/01/2006

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APPLE COMPUTER INC.

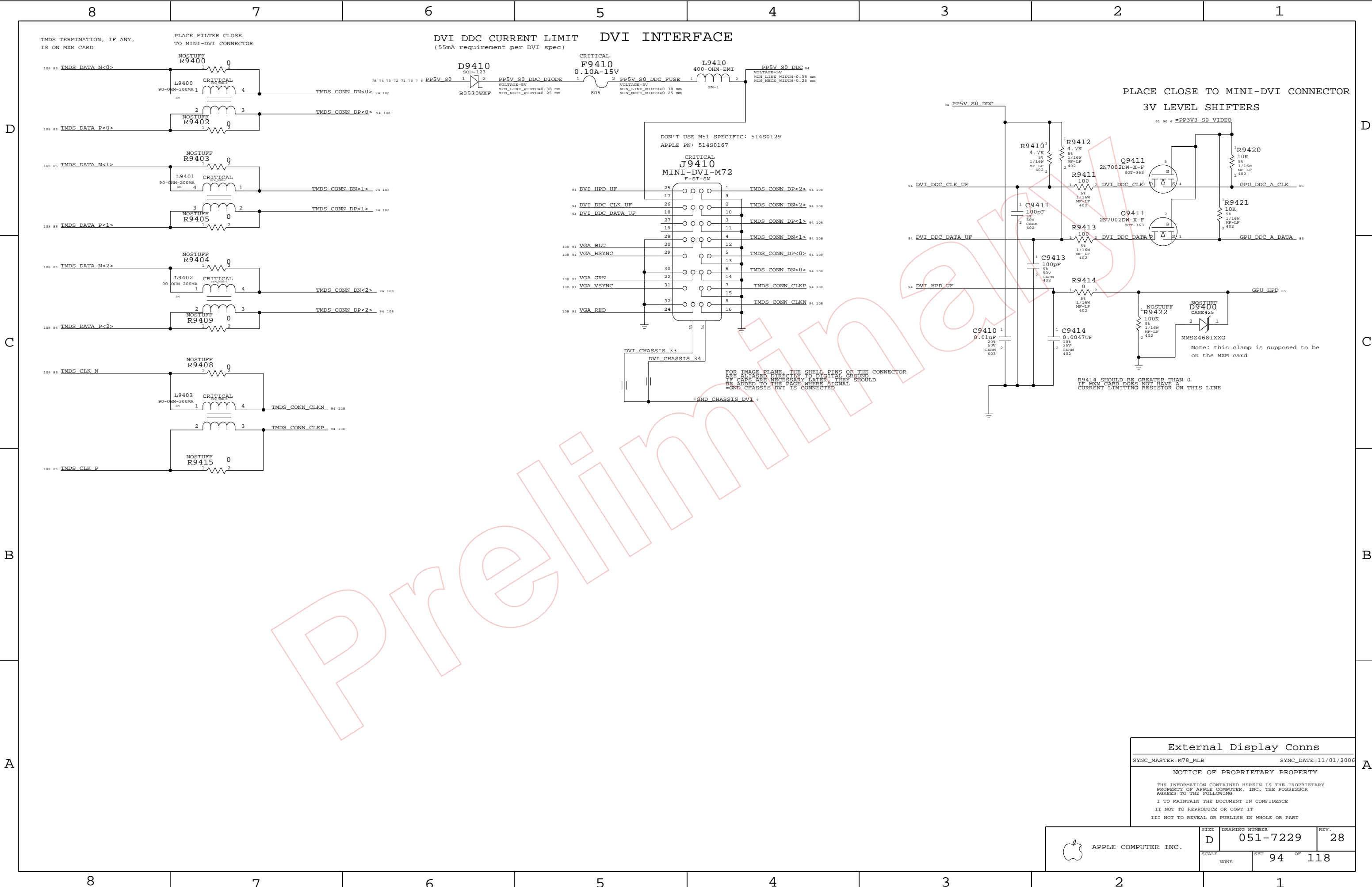
SIZE D

DRAWING NUMBER 051-7229

REV. 28

SCALE NONE

SHT 91 OF 118



External Display Conns

SYNC_MASTER=M78_MLB SYNC_DATE=11/01/2006

NOTICE OF PROPRIETARY PROPERTY

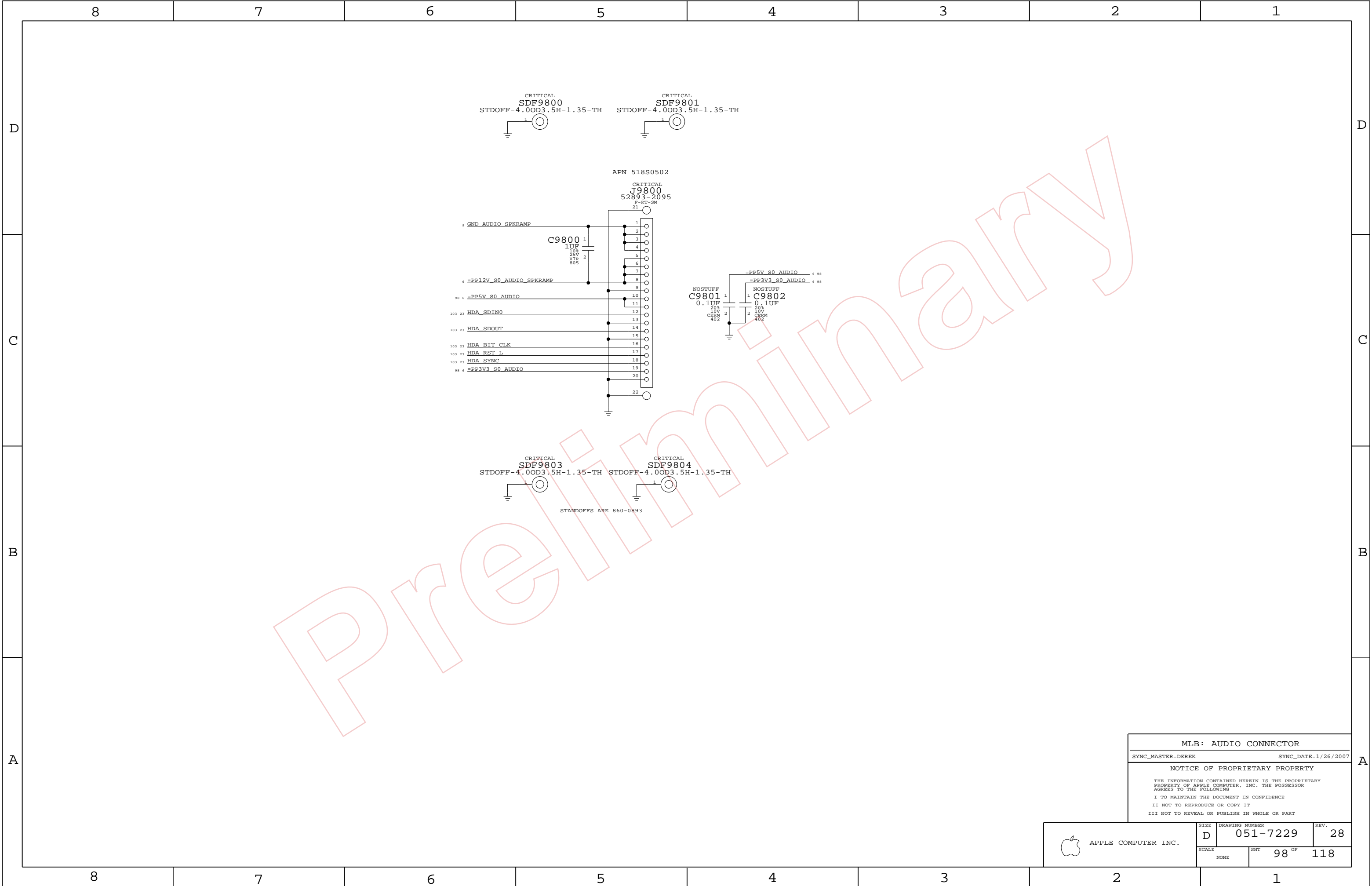
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7229	28
SCALE		SHT	OF
NONE		94	118



MLB: AUDIO CONNECTOR

SYNC_MASTER=DEREK SYNC_DATE=1/26/2007

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7229	28
SCALE		SHT	98 OF 118
NONE			

Disk Interface Constraints

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
IDE_55S	*	55_OHM_SE
SATA_55S	*	55_OHM_SE
SATA_100D	*	100_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
IDE	*	*	SPACING_0.18MM
SATA	*	*	SPACING_0.5MM

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.7 & 10.9

HD Audio Interface Constraints

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
HDA_55S	*	55_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
HDA	*	*	SPACING_0.18MM

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 10.9.1

USB 2.0 Interface Constraints

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
USB_60S	*	55_OHM_SE
USB_90D	*	90_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB	*	*	SPACING_0.5MM

DG SAYS MINIMUM SPACING 50 MILS FROM USB TO CLOCKS

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 10.13.2

Internal Interface Constraints

NET _{PHYSICAL} _TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SMB_55S	*	55_OHM_SE
SPI_55S	*	55_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SMB	*	*	SPACING_0.3MM
SPI	*	*	SPACING_0.18M

SOURCE: Santa Platform DG, Rev 1.0 (#21112), Section 10.17

ELECTRICAL_CONSTRAINT_SET		NRT_TYPE		
		PHYSICAL	SPACING	
IDE_PDD	IDE_PDD	IDE_55S	IDE	IDE_PDD<15...10> 23 44
IDE_PDD_PP	IDE_PDD_PP	IDE_55S	IDE	IDE_PDD<9> 7 23 44
IDE_PDD	IDE_PDD	IDE_55S	IDE	IDE_PDD<8...0> 23 44
IDE_PDA	IDE_PDA	IDE_55S	IDE	IDE_PDA<2...0> 23 44
IDE_PDCS1	IDE_PDCS1	IDE_55S	IDE	IDE_PDCS1 L 23 44
IDE_PDCS3	IDE_PDCS3	IDE_55S	IDE	IDE_PDCS3 L 23 44
IDE_PDIOW	IDE_PDIOW	IDE_55S	IDE	IDE_PDIOW L 23 44
IDE_PDIOR	IDE_PDIOR	IDE_55S	IDE	IDE_PDIOR L 7 23 44
IDE_PDDACK	IDE_PDDACK	IDE_55S	IDE	IDE_PDDACK L 23 44
IDE_PDDREQ	IDE_PDDREQ	IDE_55S	IDE	IDE_PDDREQ 23 44
IDE_PDIORDY	IDE_PDIORDY	IDE_55S	IDE	IDE_PDIORDY 7 23 44
IDE_IRQ14	IDE_IRQ14	IDE_55S	IDE	IDE_IRQ14 23 44
ODD_RST_L	ODD_RST_L	IDE_55S	IDE	ODD_RST_5VTOL L 24 44
SATA_A_R2D	SATA_100D	SATA	SATA_A_R2D C P	23 44
	SATA_100D	SATA	SATA_A_R2D C N	23 44
	SATA_100D	SATA	SATA_A_R2D P	45
	SATA_100D	SATA	SATA_A_R2D N	45
SATA_A_D2R	SATA_100D	SATA	SATA_A_D2R P	7 23 45
	SATA_100D	SATA	SATA_A_D2R N	7 23 45
	SATA_100D	SATA	SATA_A_D2R C P	45
	SATA_100D	SATA	SATA_A_D2R C N	45
	SATA_100D	SATA	SATA_B_R2D C P	23 45
	SATA_100D	SATA	SATA_B_R2D C N	23 45
	SATA_100D	SATA	SATA_B_D2R P	23 45
	SATA_100D	SATA	SATA_B_D2R N	23 45
SATA_RB1AS	SATA_55S		SATA_RB1AS	45
HDA_BIT_CLK	HDA_55S	HDA	HDA_BIT_CLK	23 98
	HDA_55S	HDA	HDA_BIT_CLK R	23
HDA_SYNC	HDA_55S	HDA	HDA_SYNC	23 98
	HDA_55S	HDA	HDA_SYNC R	23
HDA_RST_L	HDA_55S	HDA	HDA_RST_L	23 98
	HDA_55S	HDA	HDA_RST_L R	23
HDA_SDIN0	HDA_55S	HDA	HDA_SDIN0	23 98
	HDA_55S	HDA	HDA_SDIN_CODEC	
HDA_SDOU1	HDA_55S	HDA	HDA_SDOU1	23 98
	HDA_55S	HDA	HDA_SDOU1 R	23
USB_EXT_A	USB_90D	USB	USB_EXT_A P	24 46
	USB_90D	USB	USB_EXT_A N	24 46
	USB_90D	USB	USB_EXT_A MIXED P	
	USB_90D	USB	USB_EXT_A MIXED N	
USB_MINI	USB_90D	USB	USB_MINI P	24 34
	USB_90D	USB	USB_MINI N	24 34
	USB_90D	USB	USB_EXTD P	24 46
	USB_90D	USB	USB_EXTD N	24 46
USB_CAMERA	USB_90D	USB	USB_CAMERA P	7 24 47
	USB_90D	USB	USB_CAMERA N	7 24 47
USB_BT	USB_90D	USB	USB_BT P	7 24 47
	USB_90D	USB	USB_BT N	7 24 47
	USB_90D	USB	USB_TP1D P	24 47
	USB_90D	USB	USB_TP1D N	24 47
USB_IR	USB_90D	USB	USB_IR P	7 24 47
	USB_90D	USB	USB_IR N	7 24 47
USB_EXTR	USB_90D	USB	USB_EXTR P	24 46
	USB_90D	USB	USB_EXTR N	24 46
	USB_90D	USB	USB_EXCARD P	24 47
	USB_90D	USB	USB_EXCARD N	24 47
USB_EXTC	USB_90D	USB	USB_EXTC P	24 46
	USB_90D	USB	USB_EXTC N	24 46
USB_RB1AS	USB_60S		USB_RB1AS	24
SMB_CLK	SMB_55S	SMB	SMB_CLK	25 52
SMB_DATA	SMB_55S	SMB	SMB_DATA	25 52
SMB_ME_CLK	SMB_55S	SMB	SMB_ME_CLK	25 52
SMB_ME_DATA	SMB_55S	SMB	SMB_ME_DATA	25 52
SPI_SCL_K	SPI_55S	SPI	SPI_SCL_K R	24 61
	SPI_55S	SPI	SPI_SCL_K	7 61
	SPI_55S	SPI	SPI_A_SCL_K R	
	SPI_55S	SPI	SPI_B_SCL_K R	
SPI_SI	SPI_55S	SPI	SPI_SI R	24 61
	SPI_55S	SPI	SPI_SI	
	SPI_55S	SPI	SPI_A_SI R	61
	SPI_55S	SPI	SPI_B_SI R	
SPI_SO	SPI_55S	SPI	SPI_SO	7 24 61
	SPI_55S	SPI	SPI_A_SO R	7 61
	SPI_55S	SPI	SPI_B_SO	
	SPI_55S	SPI	SPI_B_SO R	
SPI_CE_R_L<0>	SPI_55S	SPI	SPI_CE_R_L<0>	24 61
	SPI_55S	SPI	SPI_CE_L<0>	7 61
SPI_CE_R_L<1>	SPI_55S	SPI	SPI_CE_R_L<1>	
	SPI_55S	SPI	SPI_CE_L<1>	

SB Constraints (1 of 2)	
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PCI Bus Constraints

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
PCI_55S	*	55_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCI	*	*	STANDARD

CHANGED TO 0.1MM SPACING AS THERE ARE NO PCI DEVICES

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.18.1 & 10.19

Controller Link (AMT) Constraints

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
CLINK_55S	*	55_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLINK	*	*	SPACING_0.18MM
CLINK_VREF	*	*	SPACING_0.3MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLINK_12MIL	*	=STANDARD	0.3 MM	0.125 MM	7.5 MM	=STANDARD	=STANDARD

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.27.1.5-7, 10.29 & 10.30

Ethernet (Yukon) Constraints

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
ENET_100D	*	100_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_MDI	*	*	SPACING_0.5MM
ENET_MDI	ENET_MDI_TERM	*	SPACING_0.2MM

SOURCE: Based on Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.27.1.5-7, 10.29 & 10.30

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	NET_TYPE
[]	PCT_56R	PCT	PCI AD<18..0>
[]	PCT_56R	PCT	PCI AD<19>
[]	PCT_56R	PCT	PCI AD<20>
[]	PCT_56R	PCT	PCI AD<31..21>
[]	PCT_56R	PCT	PCI PAR
[]	PCT_56R	PCT	PCI C BE L<3..0>
[]	PCT_56R	PCT	PCI IRDY L
[]	PCT_56R	PCT	PCI DEVSEL L
[]	PCT_56R	PCT	PCI PERR L
[]	PCT_56R	PCT	PCI LOCK L
[]	PCT_56R	PCT	PCI SERR L
[]	PCT_56R	PCT	PCI STOP L
[]	PCT_56R	PCT	PCI TRDY L
[]	PCT_56R	PCT	PCI FRAME L
[]	PCT_56R	PCT	PCI FW REQ L
[]	PCT_56R	PCT	PCI FW GNT L
[]	PCT_56R	PCT	PCI REQ1 L
[]	PCT_56R	PCT	PCI GNT1 L
[]	PCT_56R	PCT	PCI REQ2 L
[]	PCT_56R	PCT	PCI GNT2 L
[]	PCT_56R	PCT	INT PIROA L
[]	PCT_56R	PCT	INT PIROB L
[]	PCT_56R	PCT	INT PIROC L
[]	PCT_56R	PCT	INT PIROD L
[]	PCT_56R	PCT	INT PIROE L
[]	PCT_56R	PCT	INT PIROF L
[]	PCIE_A_R2D	PCIE_100D	PCIE MINI R2D C P
[]	PCIE_A_D2R	PCIE_100D	PCIE MINI R2D C N
[]	PCIE_B_R2D	PCIE_100D	PCIE MINI D2R P
[]	PCIE_B_D2R	PCIE_100D	PCIE ENET R2D C P
[]	PCIE_B_R2D	PCIE_100D	PCIE ENET R2D C N
[]	PCIE_B_D2R	PCIE_100D	PCIE ENET D2R P
[]	PCIE_B_R2D	PCIE_100D	PCIE ENET D2R N
[]	PCIE_B_D2R	PCIE_100D	PCIE FW R2D C P
[]	PCIE_B_D2R	PCIE_100D	PCIE FW R2D C N
[]	PCIE_B_D2R	PCIE_100D	PCIE FW D2R P
[]	PCIE_B_D2R	PCIE_100D	PCIE FW D2R N
[]	GLAN_COMP		GLAN COMP
[]	CLINK_NB	CLINK_56S	CLINK_NB_CLK
[]	CLINK_NB	CLINK_56S	CLINK_NB_DATA
[]	CLINK_NB_RESET_L	CLINK_56S	CLINK_NB_RESET_L
[]	NB_CLINK_VREF	CLINK_12MIL	NB CLINK VREF
[]	SB_CLINK_VREF0	CLINK_12MIL	SB CLINK VREF0
[]	SB_CLINK_VREF1	CLINK_12MIL	SB CLINK VREF1
[]	DWR		PPIV9R2V5_S3 ENET PHY AVDD
[]	PWR		PPIV9R2V5_S3 ENET R
[]	ENET_MDI_TERM		ENET MDI0
[]	ENET_MDI_TERM		ENET MDI1
[]	ENET_MDI_TERM		ENET MDI2
[]	ENET_MDI_TERM		ENET MDI3
[]	ENET_MDI0	ENET_100D	ENET MDI P<0>
[]	ENET_MDI1	ENET_100D	ENET MDI N<0>
[]	ENET_MDI1	ENET_100D	ENET MDI P<1>
[]	ENET_MDI1	ENET_100D	ENET MDI N<1>
[]	ENET_MDI2	ENET_100D	ENET MDI P<2>
[]	ENET_MDI2	ENET_100D	ENET MDI N<2>
[]	ENET_MDI3	ENET_100D	ENET MDI P<3>
[]	ENET_MDI3	ENET_100D	ENET MDI N<3>

SB Constraints (2 of 2)

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SCALE	

NONE

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Clock Signal Constraints

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
CLK_FSB_100D	*	100_OHM_DIFF
CLK_PCIE_100D	*	100_OHM_DIFF
CLK_MED_55S	*	55_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_FSB	*	*	CLK_SPACING_0_6MM
CLK_PCIE	*	*	CLK_SPACING_0_5MM
CLK_MED	*	*	CLK_SPACING_0_5MM

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 14.1 - 14.6

Clock Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		SPACING	
		PHYSICAL			
	CK505_CPU0	CLK_FSB 100D	CLK_FSB	CK505_CPU0_P	29 30
	CK505_CPU1	CLK_FSB 100D	CLK_FSB	CK505_CPU0_N	29 30
	CK505_NB	CLK_FSB 100D	CLK_FSB	CK505_CPU1_P	29 30
	CK505_NB	CLK_FSB 100D	CLK_FSB	CK505_CPU1_N	29 30
	CK505_I7P	CLK_FSB 100D	CLK_FSB	CK505_CPU2_I7P_SRC10_P	29 30
	CK505_I7P	CLK_FSB 100D	CLK_FSB	CK505_CPU2_I7P_SRC10_N	29 30
	CK505_PCIE0	CLK_MTD 55S	CLK_MTD	CK505_PCIE0_CLK_I7PEN	29 30
	CK505_PCIE1	CLK_MTD 55S	CLK_MTD	CK505_PCIE1_CLK	29 30
		CLK_MTD 55S	CLK_MTD	CK505_PCIE1_CLK	29 30
		CLK_MTD 55S	CLK_MTD	CK505_PCIE2_CLK	29 30
	CK505_PCIE3	CLK_MTD 55S	CLK_MTD	CK505_PCIE3_CLK	29 30
		CLK_MTD 55S	CLK_MTD	CK505_PCIE4_CLK	29 30
	CK505_PCIE5	CLK_MTD 55S	CLK_MTD	CK505_PCIE5_CLK_FCTSEL	29 30
	(CPU_BSEL0)	CLK_MTD 55S	CLK_MTD	CK505_48M_FSA	29 30
	(CPU_BSEL2)	CLK_MTD 55S	CLK_MTD	CK505_REF0_FSC	29 30
		CLK_PCIE 100D	CLK_PCIE	CK505_DOT96_27M_P	29 30
		CLK_PCIE 100D	CLK_PCIE	CK505_DOT96_27M_N	29 30
		CLK_PCIE 100D	CLK_PCIE	CK505_LVDS_P	29 30
		CLK_PCIE 100D	CLK_PCIE	CK505_LVDS_N	29 30
	CK505_SRC1	CLK_PCIE 100D	CLK_PCIE	CK505_SRC1_P	29 30
		CLK_PCIE 100D	CLK_PCIE	CK505_SRC1_N	29 30
	CK505_SRC2	CLK_PCIE 100D	CLK_PCIE	CK505_SRC2_P	29 30
		CLK_PCIE 100D	CLK_PCIE	CK505_SRC2_N	29 30
	CK505_SRC3	CLK_PCIE 100D	CLK_PCIE	CK505_SRC3_P	29 30
		CLK_PCIE 100D	CLK_PCIE	CK505_SRC3_N	29 30
	CK505_SRC4	CLK_PCIE 100D	CLK_PCIE	CK505_SRC4_P	29 30
		CLK_PCIE 100D	CLK_PCIE	CK505_SRC4_N	29 30
	CK505_SRC5	CLK_PCIE 100D	CLK_PCIE	CK505_SRC5_P	29 30
		CLK_PCIE 100D	CLK_PCIE	CK505_SRC5_N	29 30
	CK505_SRC6	CLK_PCIE 100D	CLK_PCIE	CK505_SRC6_P	29 30
		CLK_PCIE 100D	CLK_PCIE	CK505_SRC6_N	29 30
	CK505_SRC7	CLK_PCIE 100D	CLK_PCIE	CK505_SRC7_P	29 30
		CLK_PCIE 100D	CLK_PCIE	CK505_SRC7_N	29 30
	CK505_SRC8	CLK_PCIE 100D	CLK_PCIE	CK505_SRC8_P	29 30
		CLK_PCIE 100D	CLK_PCIE	CK505_SRC8_N	29 30
	(CK505_CPU1)	CLK_FSB 100D	CLK_FSB	FSB_CLK_CPU1_P	7 10 30
	(CK505_CPU1)	CLK_FSB 100D	CLK_FSB	FSB_CLK_CPU1_N	7 10 30
	(CK505_NB1)	CLK_FSB 100D	CLK_FSB	FSB_CLK_NB_P	7 14 30
	(CK505_NB1)	CLK_FSB 100D	CLK_FSB	FSB_CLK_NB_N	7 14 30
	(CK505_I7P)	CLK_FSB 100D	CLK_FSB	XDP_CLK_P	13 30 100
	(CK505_I7P)	CLK_FSB 100D	CLK_FSB	XDP_CLK_N	13 30 100
	(CK505_PCIE0)	CLK_MTD 55S	CLK_MTD	PCI_CLK33M_LPCPLUS	7 30 61
	(CK505_PCIE1)	CLK_MTD 55S	CLK_MTD	PCI_CLK33M_SB	7 24 30
	(CK505_PCIE2)	CLK_MTD 55S	CLK_MTD	PCI_CLK33M_TPM	
	(CK505_PCIE3)	CLK_MTD 55S	CLK_MTD	PCI_CLK33M_SMC	7 30 49
				CK505_PCIE4 is project-specific	
				CK505_PCIE5 is project-specific	
	(CPU_BSEL0)	CLK_MTD 55S	CLK_MTD	SB_CLK48M_USBCLE	7 25 30
	(CPU_BSEL2)	CLK_MTD 55S	CLK_MTD	SB_CLK14P3M_TIMER	7 25 30
	(CPU_BSEL0)	CLK_MTD 55S	CLK_MTD	CK505_FSA	30
	(CPU_BSEL2)	CLK_MTD 55S	CLK_MTD	CK505_FSC	30
	(CK505_SRC1)	CLK_PCIE 100D	CLK_PCIE	GPU_CLK100M_PCIE_P	30 85
	(CK505_SRC1)	CLK_PCIE 100D	CLK_PCIE	GPU_CLK100M_PCIE_N	30 85
	(CK505_SRC2)	CLK_PCIE 100D	CLK_PCIE	SB_CLK100M_DMI_P	7 24 30
	(CK505_SRC2)	CLK_PCIE 100D	CLK_PCIE	SB_CLK100M_DMI_N	7 24 30
	(CK505_SRC3)	CLK_PCIE 100D	CLK_PCIE	PCIE_CLK100M_FW_P	7 30 40
	(CK505_SRC3)	CLK_PCIE 100D	CLK_PCIE	PCIE_CLK100M_FW_N	7 30 40
	(CK505_SRC4)	CLK_PCIE 100D	CLK_PCIE	SB_CLK100M_SATA_P	7 23 30
	(CK505_SRC4)	CLK_PCIE 100D	CLK_PCIE	SB_CLK100M_SATA_N	7 23 30
	(CK505_SRC5)	CLK_PCIE 100D	CLK_PCIE	NB_CLK100M_PCIE_P	7 16 30
	(CK505_SRC5)	CLK_PCIE 100D	CLK_PCIE	NB_CLK100M_PCIE_N	7 16 30
	(CK505_SRC6)	CLK_PCIE 100D	CLK_PCIE	PCIE_CLK100M_MINI_P	30 34
	(CK505_SRC6)	CLK_PCIE 100D	CLK_PCIE	PCIE_CLK100M_MINI_N	30 34
	(CK505_SRC8)	CLK_PCIE 100D	CLK_PCIE	PCIE_CLK100M_ENET_P	7 30 37
	(CK505_SRC8)	CLK_PCIE 100D	CLK_PCIE	PCIE_CLK100M_ENET_N	7 30 37

Clock Constraints

SYNC_MASTER=T9_MLB	SYNC_DATE=09/27/2006
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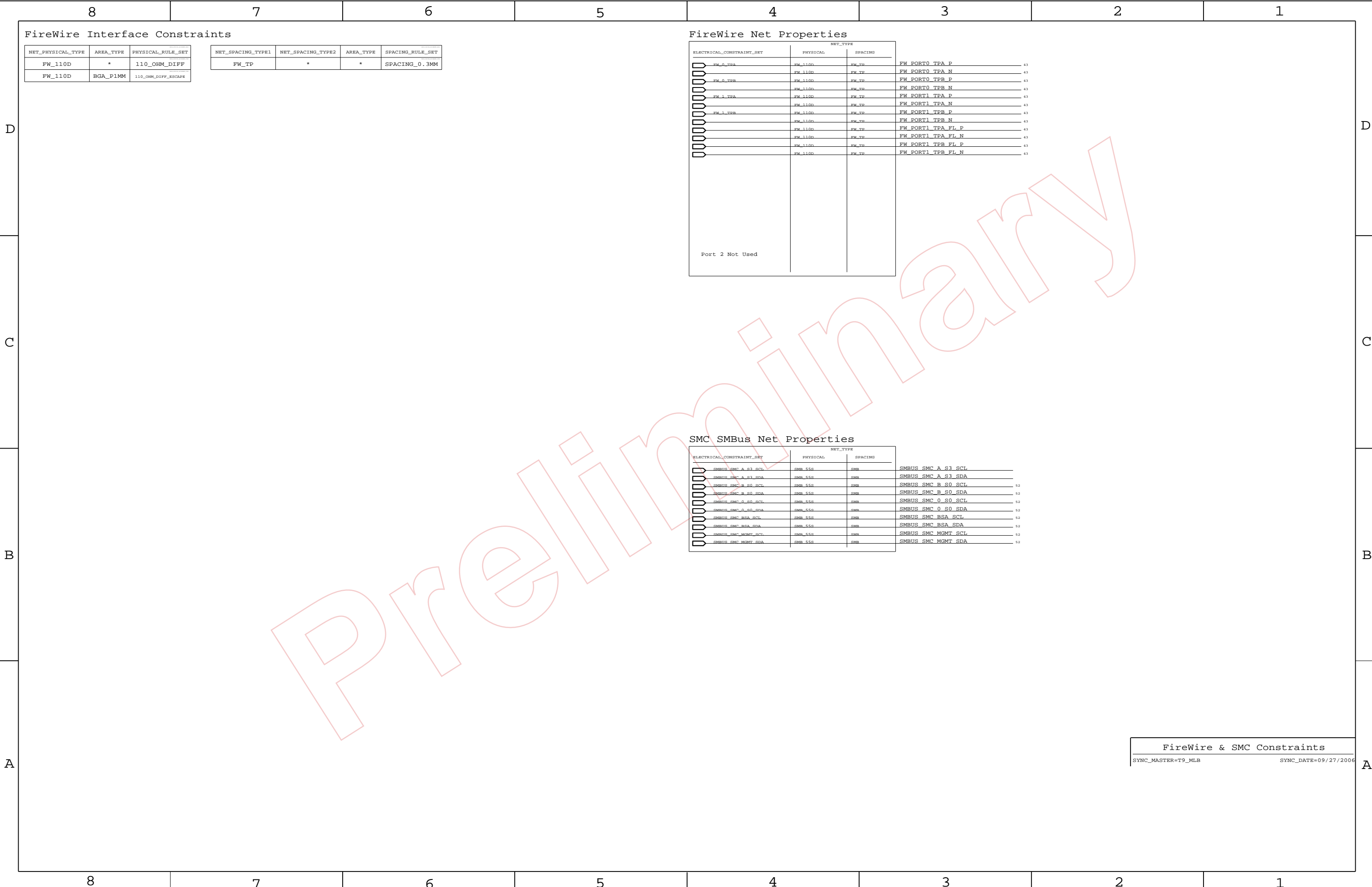
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NONE	105	118
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Preliminary

8		7		6		5		4		3		2		1	
M72/M78 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS															
BOARD LAYERS						BOARD AREAS			BOARD UNITS (MIL or MM)		ALLEGRO VERSION				
TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, BOTTOM						NO_TYPE, BGA_P1MM			MM		15.5.1				
PHYSICAL_RULE_SET		LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP							
DEFAULT		*	Y	=55_OHM_SE	=55_OHM_SE	4 MM	0 MM	0 MM							
STANDARD		*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT							
DEFAULT		TOP, BOTTOM	Y	=55_OHM_SE	0.100 MM	3 MM	0 MM	0 MM							
PHYSICAL_RULE_SET		LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP							
55_OHM_SE		TOP, BOTTOM	Y	0.125 MM	0.125 MM										
55_OHM_SE		*	Y	0.100 MM	0.100 MM	=STANDARD	=STANDARD	=STANDARD							
PHYSICAL_RULE_SET		LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP							
40_OHM_SE		TOP, BOTTOM	Y	0.225 MM	0.225 MM										
40_OHM_SE		*	Y	0.185 MM	0.185 MM	=STANDARD	=STANDARD	=STANDARD							
PHYSICAL_RULE_SET		LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP							
45_OHM_SE		TOP, BOTTOM	Y	0.185 MM	0.185 MM										
45_OHM_SE		*	Y	0.150 MM	0.150 MM	=STANDARD	=STANDARD	=STANDARD							
PHYSICAL_RULE_SET		LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP							
27P4_OHM_SE		TOP, BOTTOM	Y	0.340 MM	0.340 MM										
27P4_OHM_SE		*	Y	0.265 MM	0.265 MM	=STANDARD	=STANDARD	=STANDARD							
PHYSICAL_RULE_SET		LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP							
70_OHM_DIFF		*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD							
70_OHM_DIFF		ISL3, ISL6	Y	0.180 MM	0.180 MM		0.120 MM	0.120 MM							
70_OHM_DIFF		TOP, BOTTOM	Y	0.215 MM	0.215 MM		0.125 MM	0.125 MM							
PHYSICAL_RULE_SET		LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP							
85_OHM_DIFF		*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD							
85_OHM_DIFF		ISL3, ISL6	Y	0.120 MM	0.120 MM		0.130 MM	0.130 MM							
85_OHM_DIFF		TOP, BOTTOM	Y	0.145 MM	0.145 MM		0.125 MM	0.125 MM							
PHYSICAL_RULE_SET		LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP							
90_OHM_DIFF		*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD							
90_OHM_DIFF		ISL3, ISL6	Y	0.125 MM	0.125 MM		0.200 MM	0.200 MM							
90_OHM_DIFF		TOP, BOTTOM	Y	0.145 MM	0.145 MM		0.175 MM	0.175 MM							
PHYSICAL_RULE_SET		LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP							
100_OHM_DIFF		*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD							
100_OHM_DIFF		ISL3, ISL6	Y	0.095 MM	0.095 MM		0.205 MM	0.205 MM							
100_OHM_DIFF		TOP, BOTTOM	Y	0.115 MM	0.115 MM		0.180 MM	0.180 MM							
PHYSICAL_RULE_SET		LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP							
110_OHM_DIFF		*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD							
110_OHM_DIFF		ISL3, ISL6	Y	0.085 MM	0.085 MM		0.330 MM	0.330 MM							
110_OHM_DIFF		TOP, BOTTOM	Y	0.105 MM	0.100 MM		0.280 MM	0.280 MM							
PHYSICAL_RULE_SET		LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP							
1:1_DIFFPAIR		*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM							
SPACING_RULE_SET				LAYER	LINE-TO-LINE SPACING	WEIGHT	NET_SPACING_TYPE1		NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET				
DEFAULT				*	0.1 MM	?	*		*	BGA_P1MM	BGA_P1MM				
STANDARD				*	=DEFAULT	?	MEM_CLK		*	BGA_P1MM	BGA_P2MM				
BGA_P1MM				*	=DEFAULT	?	CLK_FSB		*	BGA_P1MM	BGA_P2MM				
BGA_P2MM				*	=DEFAULT	?	CLK_PCIE		*	BGA_P1MM	BGA_P2MM				
BGA_P3MM				*	=DEFAULT	?	CLK_MED		*	BGA_P1MM	BGA_P2MM				
SPACING_RULE_SET				LAYER	LINE-TO-LINE SPACING	WEIGHT	FSB_DSTB		FSB_DSTB	BGA_P1MM	BGA_P3MM				
SPACING_0.15MM				*	0.15 MM	?									
SPACING_0.18MM				*	0.18 MM	?									
SPACING_0.2MM				*	0.2 MM	?									
SPACING_0.25MM				*	0.25 MM	?									
SPACING_0.3MM				*	0.3 MM	?									
SPACING_0.4MM				*	0.4 MM	?									
SPACING_0.5MM				*	0.5 MM	?									
SPACING_0.6MM				*	0.6 MM	?									
SWITCHNODE				*	0.6 MM	1000									
SWITCHNODE				TOP, BOTTOM	0.2 MM	1000									
M72/M78 RULE DEFINITIONS															
SYNC_MASTER=T9_MLB SYNC_DATE=09/27/2006															
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 APPLE COMPUTER INC.										SIZE D		DRAWING NUMBER 051-7229		REV. 28	
										SCALE NONE		SHT 109		OF 118	
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D	C7290	CAP_402	m78[72C4]	C7300	CAP_P_CASE-D2-SM	m78[73C8]	C7301	CAP_805	m78[73C8]	C7302	CAP_402	m78[73B7]	C7303	CAP_P_CASE-D2-SM	m78[73C7]	C7304	CAP_805	m78[73C8]	C7310	CAP_603	m78[73C7]	C7324	CAP_402	m78[73B7]	C7330	CAP_603-1	m78[73D6]	C7331	CAP_603	m78[73C6]	C7332	CAP_402	m78[73B5]	C7335	CAP_402	m78[73B6]	C7340	CAP_P_TH	m78[73D7]	C7341	CAP_1206-1	m78[73D7]	C7342	CAP_1206-1	m78[73D6]	C7345	CAP_402	m78[73B3]	C7360	CAP_603	m78[73D2]	C7361	CAP_603	m78[73C2]	C7364	CAP_402	m78[73B2]	C7370	CAP_402	m78[73B2]	C7372	CAP_402	m78[73B4]	C7381	CAP_1206-1	m78[73D2]	C7382	CAP_1206-1	m78[73D2]	C7390	CAP_P_CASE-D2-SM	m78[73C1]	C7391	CAP_P_CASE-D2-SM	m78[73C2]	C7392	CAP_805	m78[73C1]	C7393	CAP_805	m78[73C1]	C7400	CAP_P_CASE-D2-SM	m78[74C8]	C7401	CAP_805	m78[74C8]	C7402	CAP_402	m78[74B7]	C7403	CAP_P_CASE-D2-SM	m78[74C7]	C7404	CAP_805	m78[74C8]	C7410	CAP_603	m78[74C7]	C7424	CAP_402	m78[74B7]	C7430	CAP_603-1	m78[74D6]	C7431	CAP_603	m78[74C6]	C7432	CAP_402	m78[74B5]	C7435	CAP_402	m78[74B6]	C7440	CAP_P_TH	m78[74D7]	C7441	CAP_1206-1	m78[74D7]	C7442	CAP_1206-1	m78[74D6]	C7445	CAP_402	m78[74B3]	C7460	CAP_603-1	m78[74D2]	C7461	CAP_603	m78[74C2]	C7464	CAP_402	m78[74B2]	C7470	CAP_402	m78[74B2]	C7472	CAP_402	m78[74B4]	C7480	CAP_P_TH	m78[74D3]	C7481	CAP_1206-1	m78[74D2]	C7482	CAP_1206-1	m78[74D2]	C7490	CAP_P_TH	m78[74C2]	C7491	CAP_P_TH	m78[74C1]	C7492	CAP_805	m78[74C1]	C7493	CAP_805	m78[74C1]	C7500	CAP_603	m78[75D5]	C7501	CAP_603	m78[75D6]	C7502	CAP_603	m78[75D6]	C7503	CAP_402	m78[75C2]	C7506	CAP_402	m78[75C8]	C7507	CAP_402	m78[75C6]	C7508	CAP_603	m78[75C7]	C7509	CAP_402	m78[75D4]	C7510	CAP_402	m78[75C5]	C7530	CAP_P_TH	m78[75D5]	C7531	CAP_603	m78[75D4]	C7532	CAP_P_TH	m78[75D5]	C7533	CAP_1206-1	m78[75D5]	C7534	CAP_1206-1	m78[75D4]	C7540	CAP_805	m78[75C3]	C7541	CAP_805	m78[75C3]	C7542	CAP_P_CASE-D2-SM	m78[75C2]	C7543	CAP_P_CASE-D2-SM	m78[75C2]	C7544	CAP_P_CASE-D2-SM	m78[75C2]	C7550	CAP_402	m78[75B4]	C7551	CAP_805-1	m78[75A6]	C7552	CAP_805-1	m78[75A4]	C7553	CAP_402	m78[75A6]	C7555	CAP_P_CASE-C3	m78[75A4]	C7559	CAP_603	m78[75B5]	C7560	CAP_402	m78[75D8]	C7564	CAP_402	m78[75C3]	C7600	CAP_603	m78[76C4]	C7601	CAP_603	m78[76A4]	C7602	CAP_402	m78[76A4]	C7604	CAP_402	m78[76A3]	C7605	CAP_402	m78[76B5]	C7607	CAP_402	m78[76A3]	C7608	CAP_402	m78[76D2]	C7609	CAP_402	m78[76D7]	C7612	CAP_603	m78[76A7]	C7613	CAP_402	m78[76A7]	C7621	CAP_402	m78[76B6]	C7622	CAP_402	m78[76C5]	C7624	CAP_402	m78[76C6]	C7625	CAP_402	m78[76B6]	C7626	CAP_402	m78[76B6]	C7628	CAP_402	m78[76B7]	C7629	CAP_402	m78[76B7]	C7630	CAP_402	m78[76A5]	C7631	CAP_402	m78[76C7]	C7632	CAP_402	m78[76C2]	C7640	CAP_1206-1	m78[76D6]	C7641	CAP_1206-1	m78[76D6]	C7642	CAP_1206-1	m78[76D6]	C7643	CAP_1206-1	m78[76D6]	C7650	CAP_805	m78[76B7]	C7651	CAP_P_CASE-D3L	m78[76B8]	C7652	CAP_P_CASE-D3L	m78[76B8]	C7661	CAP_402	m78[76B3]	C7662	CAP_402	m78[76C4]	C7664	CAP_402	m78[76C3]	C7665	CAP_402	m78[76B4]	C7666	CAP_402	m78[76B3]	C7668	CAP_402	m78[76B2]	C7669	CAP_402	m78[76B2]	C7670	CAP_402	m78[76B4]	C7680	CAP_1206-1	m78[76D3]	C7681	CAP_1206-1	m78[76D4]	C7682	CAP_P_SM-1	m78[76D4]	C7689	CAP_402	m78[76B4]	C7690	CAP_805	m78[76B2]	C7691	CAP_P_CASE-D3L	m78[76B1]	C7692	CAP_P_CASE-D3L	m78[76B1]	C7693	CAP_P_CASE-D3L	m78[76B1]
	C7700	CAP_805	m78[77C6]	C7701	CAP_402	m78[77C5]	C7702	CAP_402	m78[77B3]	C7705	CAP_805	m78[77B3]	C7706	CAP_805	m78[77B3]	C7707	CAP_805	m78[77B3]	C7710	CAP_805	m78[77D6]	C7712	CAP_402	m78[77D4]	C7715	CAP_805	m78[77D3]	C7800	CAP_402	m78[78D4]	C7801	CAP_402	m78[78D4]	C7810	CAP_402	m78[78D6]	C7811	CAP_402	m78[78D7]	C7850	CAP_402	m78[78C4]	C7851	CAP_402	m78[78C4]	C7890	CAP_805	m78[78D2]	C7891	CAP_402	m78[78D2]	C7895	CAP_402	m78[78B7]	C7896	CAP_402	m78[78A6]	C7899	CAP_402	m78[78B6]	C8400	CAP_P_SM-LF	m78[84C5]	C8401	CAP_805	m78[84C7]	C8420	CAP_402	m78[84C7]	C8421	CAP_402	m78[84C7]	C8422	CAP_402	m78[84C7]	C8423	CAP_402	m78[84C7]	C8424	CAP_402	m78[84B7]	C8425	CAP_402	m78[84B7]	C8426	CAP_402	m78[84B7]	C8427	CAP_402	m78[84B7]	C8428	CAP_402	m78[84B7]	C8429	CAP_402	m78[84B7]	C8430	CAP_402	m78[84B7]	C8431	CAP_402	m78[84B7]	C8432	CAP_402	m78[84B7]	C8433	CAP_402	m78[84B7]	C8434	CAP_402	m78[84B7]	C8435	CAP_402	m78[84B7]	C8436	CAP_402	m78[84B7]	C8437	CAP_402	m78[84B7]	C8438	CAP_402	m78[84B7]	C8439	CAP_402	m78[84B7]	C8440	CAP_402	m78[84B7]	C8441	CAP_402	m78[84A7]	C8442	CAP_402	m78[84A7]	C8443	CAP_402	m78[84A7]	C8444	CAP_402	m78[84A7]	C8445	CAP_402	m78[84A7]	C8446	CAP_402	m78[84A7]	C8447	CAP_402	m78[84A7]	C8448	CAP_402	m78[84A7]	C8449	CAP_402	m78[84A7]	C8450	CAP_402	m78[84A7]	C8451	CAP_402	m78[84A7]	C8500	CAP_805	m78[85A5]	C8570	CAP_402	m78[85D2]	C9000	CAP_603-1	m78[90C7]	C9001	CAP_402	m78[90C5]	C9010	CAP_402	m78[90A8]	C9020	CAP_1210	m78[90C5]	C9130	CAP_402	m78[91B7]	C9131	CAP_805-1	m78[91B7]	C9140	CAP_402	m78[91A5]	C9141	CAP_402	m78[91B5]	C9142	CAP_402	m78[91B5]	C9143	CAP_402	m78[91A6]	C9144	CAP_402	m78[91B6]	C9145	CAP_402	m78[91B6]	C9160	CAP_402	m78[91B4]	C9161	CAP_402	m78[91B4]	C9162	CAP_402	m78[91A2]	C9163	CAP_402	m78[91A2]	C9410	CAP_603	m78[94C3]	C9411	CAP_402	m78[94D3]	C9413	CAP_402	m78[94C2]	C9414	CAP_402	m78[94C2]	C9415	CAP_805	m78[98C5]	C9800	CAP_805	m78[98C5]	C9801	CAP_402	m78[98C4]	C9802	CAP_402	m78[98C4]	D2185	DIODE_SCHOT_SOT23	m78[21C4]	D2186	DIODE_SCHOT_SOT23	m78[21B4]	D2702	DIODE_SCHOT_6PB_SOT-363	m78[27D8 27D8]																																																																																																																											
	D2800	DIODE_SCHOT_6PB_SOT-363	m78[28D6]	D4390	ZENER_SOT23	m78[43A6]	D4600	DIODE_SCHOT_3P_A_SC-75	m78[46C2]	D4601	DIODE_SCHOT_3P_A_SC-75	m78[46B5]	D4602	DIODE_SCHOT_3P_A_SC-75	m78[46A5]	D5350	DIODE_3P_2NC_SOT23-L																																																																																																																																																																																																																																																																																																																																																																			

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D	R5055	RES_402	m78[50A3]	R7104	RES_402	m78[71C1]	R7850	RES_402	m78[78C5]	U7056	MC74VHC1G08_SOT23-5- LF	m78[70C2]	D				C	U7100	ISL6260C_QFN	m78[71C6]				B				A			
	R5056	RES_402	m78[50A3]	R7105	RES_402	m78[71B2]	R7851	RES_402	m78[78C5]	U7101	ISL6208_QFN	m78[71D5]						U7102	ISL6208_QFN	m78[71C5]											
	R5057	RES_402	m78[50A6]	R7106	RES_603	m78[71B2]	R7870	RES_402	m78[78B7]	U7201	ISL6208_QFN	m78[72C7]						U7300	ISL6539_SSOP	m78[73C5]											
	R5058	RES_402	m78[50A5]	R7107	RES_402	m78[71B1]	R7871	RES_402	m78[78B7]	U7400	ISL6539_SSOP	m78[74C5]						U7500	ISL6269_QFN	m78[75D6]											
	R5059	RES_402	m78[50A4]	R7108	RES_402	m78[71C8]	R7888	RES_402	m78[78C1]	U7501	SN74LVCL1G07_SC70	m78[75D8]						U7600	LTC3728L_QFN	m78[76C5]											
	R5070	RES_402	m78[50D2]	R7109	RES_402	m78[71B7]	R7889	RES_402	m78[78C2]	U7601	COMPARATOR_LM393A_SOI	m78[76D6 76A7]-1-LF						U7710	TPS62050_MSOP	m78[77D5]											
	R5071	RES_402	m78[50D3]	R7110	RES_402	m78[71B7]	R7891	RES_402	m78[78D3]	U7750	TPS62510_BQA	m78[77B4]						U8570	EEPROM_M24C02_S08	m78[85D2]											
	R5078	RES_402	m78[50D1]	R7111	RES_402	m78[71B8]	R7892	RES_402	m78[78D2]	U9130	VIDEO_TS3V330_SOP	m78[91B7]						U9160	74LVCL1G125LF_SOT23-5	m78[91B4]											
	R5080	RES_402	m78[50B1]	R7112	RES_402	m78[71D7]	R7893	RES_402	m78[78D3]	U9161	74LVCL1G125LF_SOT23-5	m78[91A4]						VR5065	VREF_REF3133_SOT23-3	m78[50B8]											
	R5082	RES_402	m78[50B1]	R7114	RES_402	m78[71B7]	R7894	RES_805	m78[78D1]	XW4900	SHORT_SM	m78[49C2]						XW4900	SHORT_SM	m78[49C2]											
C	R5083	RES_402	m78[50A1]	R7115	RES_402	m78[71B4]	R7895	RES_402	m78[78A7]	XW5309	SHORT_SM	m78[53D7]	C				B	XW5350	SHORT_SM	m78[53C3]				A							
	R5084	RES_402	m78[50A1]	R7116	RES_402	m78[71B4]	R7896	RES_402	m78[78A6]	XW5500	SHORT_SM	m78[55A4]						XW5501	SHORT_SM	m78[55A4]											
	R5086	RES_402	m78[50A1]	R7117	RES_402	m78[71B5]	R7897	RES_402	m78[78B6]	XW5502	SHORT_SM	m78[55A4]						XW5502	SHORT_SM	m78[55A4]											
	R5087	RES_402	m78[50B1]	R7118	RES_402	m78[71B5]	R7898	RES_402	m78[78B6]	XW7100	SHORT_SM	m78[71A6]						XW7101	SHORT_SM	m78[71B2]											
	R5088	RES_402	m78[50A1]	R7119	RES_402	m78[71C8]	R8500	RES_402	m78[85C7]	XW7102	SHORT_SM	m78[71B1]						XW7103	SHORT_SM	m78[71D2]											
	R5090	RES_402	m78[50B1]	R7120	RES_402	m78[71D7]	R8501	RES_402	m78[85C5]	XW7104	SHORT_SM	m78[71D1]						XW7203	SHORT_SM	m78[72C3]											
	R5091	RES_402	m78[50B1]	R7121	RES_402	m78[71D7]	R8502	RES_402	m78[85C7]	XW7204	SHORT_SM	m78[72C2]						XW7300	SHORT_SM	m78[73B4]											
	R5092	RES_402	m78[50B1]	R7122	RES_402	m78[71A4]	R8503	RES_402	m78[85A4]	XW7400	SHORT_SM	m78[74B4]						XW7400	SHORT_SM	m78[74B4]											
	R5093	RES_402	m78[50B1]	R7123	RES_402	m78[71A4]	R8505	RES_402	m78[85B4]	XW7500	SHORT_SM	m78[75C5]						XW7500	SHORT_SM	m78[75C5]											
	R5094	RES_402	m78[50B1]	R7126	THERMISTHER_402	m78[71C8]	R8570	RES_402	m78[85D3]	XW7600	SHORT_SM	m78[76A5]						XW7600	SHORT_SM	m78[76A5]											
B	R5096	RES_402	m78[50B1]	R7127	RES_402	m78[71C7]	R9000	RES_402	m78[90C8]	Y2900	CRYSTAL_4PIN_SM-LF	m78[28C7]	B				A	Y2901	CRYSTAL_5X3.2-SM	m78[29C6]											
	R5190	RES_402	m78[51B2]	R7130	RES_402	m78[71B4]	R9001	RES_402	m78[90C7]	Y2901	CRYSTAL_5X3.2-SM	m78[29C6]						Y3750	CRYSTAL_SM-3-LF	m78[37B5]											
	R5191	RES_402	m78[51C3]	R7131	THERMISTHER_0603-LF	m78[71B4]	R9002	RES_805	m78[90C8]	Y3750	CRYSTAL_SM-3-LF	m78[37B5]						Y4000	CRYSTAL_HC49-USMD	m78[40B7]											
	R5192	RES_402	m78[51C4]	R7140	RES_603	m78[71B1]	R9003	RES_805	m78[90C8]	Y4000	CRYSTAL_HC49-USMD	m78[40B7]						Y5020	CRYSTAL_SM-4	m78[50C8]											
	R5200	RES_402	m78[52D7]	R7141	RES_603	m78[71C1]	R9070	RES_402	m78[90B7]	ZH500	HOLE_VIA	m78[7C1]						ZH501	HOLE_VIA	m78[7C1]											
	R5201	RES_402	m78[52D7]	R7142	RES_402	m78[71D4]	R9074	RES_402	m78[90B2]	ZH502	HOLE_VIA	m78[7C1]						ZH503	HOLE_VIA	m78[7C1]											
	R5230	RES_402	m78[52A7]	R7143	RES_402	m78[71C4]	R9075	RES_402	m78[90B2]	ZH504	HOLE_VIA	m78[7B1]						ZH505	HOLE_VIA	m78[7B1]											
	R5231	RES_402	m78[52A7]	R7147	RES_402	m78[71D6]	R9090	RES_805	m78[90C6]	ZH506	HOLE_VIA	m78[7B1]						ZH507	HOLE_VIA	m78[7B1]											
	R5250	RES_402	m78[52D4]	R7199	RES_402	m78[71C7]	R9099	RES_402	m78[90C8]	ZH508	HOLE_VIA	m78[7B1]						ZH508	HOLE_VIA	m78[7B1]											
	R5251	RES_402	m78[52D4]	R7200	RES_402	m78[72C3]	R9140	RES_402	m78[91A6]	ZH509	HOLE_VIA	m78[7B1]						ZH510	HOLE_VIA	m78[7C1]											
A	R5260	RES_402	m78[52C4]	R7201	RES_603	m78[72B3]	R9141	RES_402	m78[91B6]	ZH511	HOLE_VIA	m78[7C1]	A					ZH512	HOLE_VIA	m78[7C1]											
	R5261	RES_402	m78[52C4]	R7203	RES_1206	m78[72C3]	R9142	RES_402	m78[91B6]	ZH513	HOLE_VIA	m78[7C1]						ZH514	HOLE_VIA	m78[7B1]											
	R5270	RES_402	m78[52D2]	R7204	RES_402	m78[72C2]	R9160	RES_402	m78[91B3]	ZH515	HOLE_VIA	m78[7B1]						ZH516	HOLE_VIA	m78[7B1]											
	R5271	RES_402	m78[52D2]	R7241	RES_603	m78[72C2]	R9161	RES_402	m78[91A3]	ZH517	HOLE_VIA	m78[7B1]						ZH518	HOLE_VIA	m78[7B1]											
	R5280	RES_402	m78[52C2]	R7250	RES_402	m78[72C5]	R9400	RES_402	m78[94D7]	ZH519	HOLE_VIA	m78[7B1]						ZH520	HOLE_VIA	m78[7B1]											
	R5281	RES_402	m78[52C2]	R7300	RES_402	m78[73B7]	R9403	RES_402	m78[94D7]	ZH521	HOLE_VIA	m78[7C1]						ZH522	HOLE_VIA	m78[7C1]											
	R5290	RES_402	m78[52B2]	R7301	RES_402	m78[73B7]	R9404	RES_402	m78[94C7]	ZH523	HOLE_VIA	m78[7C1]						ZH524	HOLE_VIA	m78[7B1]											
	R5291	RES_402	m78[52B2]	R7306	RES_1206	m78[73C7]	R9405	RES_402	m78[94C7]	ZH525	HOLE_VIA	m78[7B1]						ZH526	HOLE_VIA	m78[7B1]											
	R5309	RES_402	m78[53D7]	R7310	RES_1206	m78[73A3]	R9408	RES_402	m78[94C7]	ZH527	HOLE_VIA	m78[7B1]						ZH528	HOLE_VIA	m78[7B1]											
	R5339	RES_402	m78[53B7]	R7311	RES_1206	m78[73A3]	R9408	RES_402	m78[94C7]	ZH529	HOLE_VIA	m78[7B1]						ZH530	HOLE_VIA	m78[7B1]											